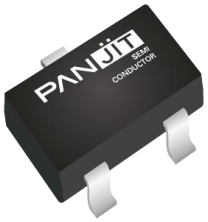
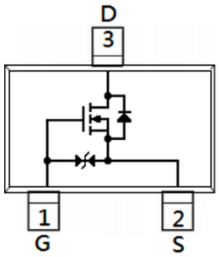
2N7002K

60V N-Channel Enhancement Mode MOSFET – ESD Protected

Voltage 60 V **Current** 300mA

SOT-23





Features

- $R_{DS(ON)}$, V_{GS}@10V, I_D@500mA<3Ω
- $R_{DS(ON)}$, V_{GS}@4.5V, I_D@200mA<4Ω
- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Very Low Leakage Current In Off Condition
- Specially Designed for Battery Operated Systems, Solid-State Relays Drivers: Relay, Displays, Memories, etc
- ESD Protected 2KV HBM
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : SOT-23 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0084 grams

Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current(Note 4)		I_D	300	mA
Pulsed Drain Current(Note 1)		I_{DM}	2000	
Power Dissipation	T_A=25°C	P_D	500	mW
	Derate above 25°C		4	mW/°C
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~150	°C
Typical Thermal Resistance - Junction to Ambient(Note 3,4)		$R_{\theta JA}$	250	°C/W

PANJIT SEMI CONDUCTOR

2N7002K

Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=10uA	60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	1	-	2.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=500mA	-	-	3	Ω
		V_{GS}=4.5V,I_D=200mA	-	-	4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±10	
Forward Transconductance	g_{fs}	V_{DS}=15V, I_D=250mA	100	-	-	mS
Dynamic(Note 5)						
Total Gate Charge	Q_g	V_{DS}=15V, I_D=250mA, V_{GS}=5V(Note 1,2)	-	0.8	-	nC
Gate-Source Charge	Q_{gs}		-	0.35	-	
Gate-Drain Charge	Q_{gd}		-	0.2	-	
Input Capacitance	Ciss	V_{DS}=25V, V_{GS}=0V, f=1MHZ	-	35	-	pF
Output Capacitance	Coss		-	13	-	
Reverse Transfer Capacitance	Crss		-	8	-	
Turn-On Delay Time	$td_{(on)}$	V_{DD}=30V, I_D=200mA, V_{GS}=10V, R_G=10Ω(Note 1,2)	-	2.7	-	ns
Turn-On Rise Time	tr		-	19	-	
Turn-Off Delay Time	$td_{(off)}$		-	15	-	
Turn-Off Fall Time	tf		-	23	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	300	mA
Diode Forward Voltage	V_{SD}	I_S=200mA, V_{GS}=0V	-	0.82	1.3	V

NOTES:

1. Pulse width≤300us, Duty cycle≤2%.
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

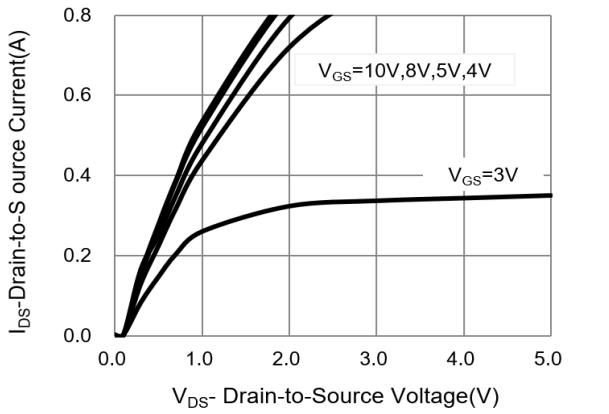

Fig.1 On-Region Characteristics

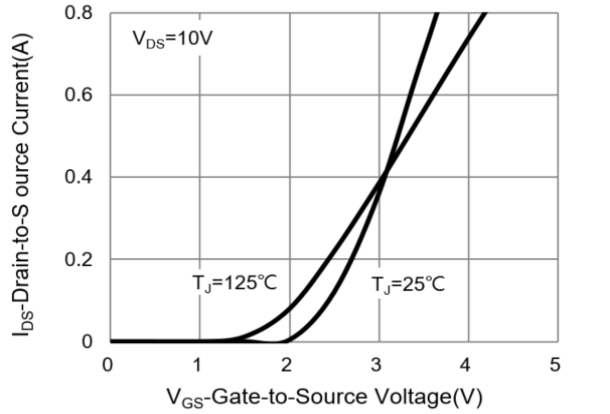

Fig.2 Transfer Characteristics

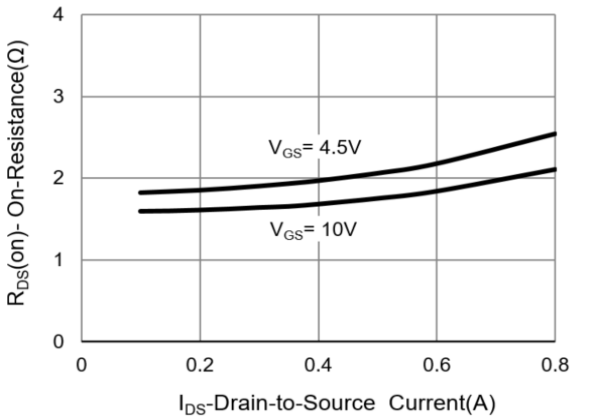

Fig.3 On-Resistance vs. Drain Current

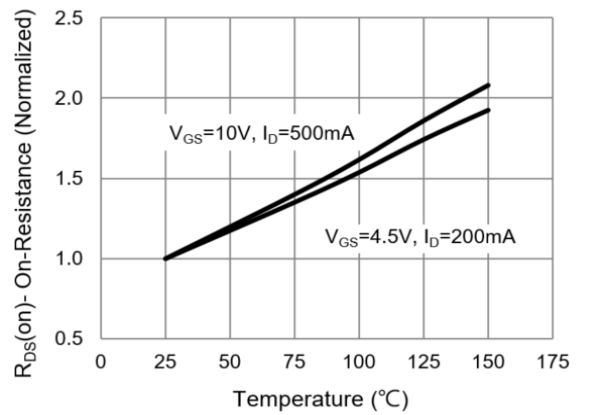

Fig.4 On-Resistance vs. Junction temperature

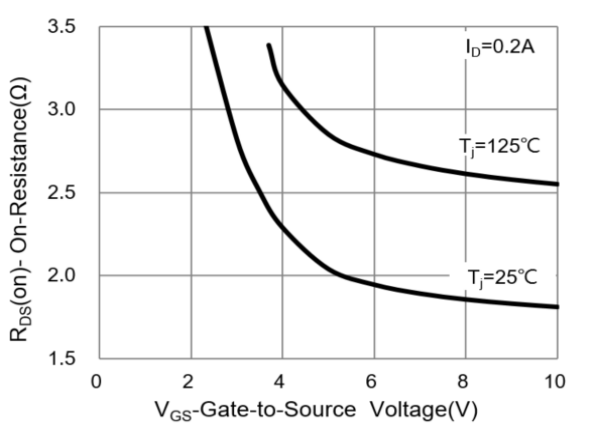

Fig.5 On-Resistance Variation with V_{GS}

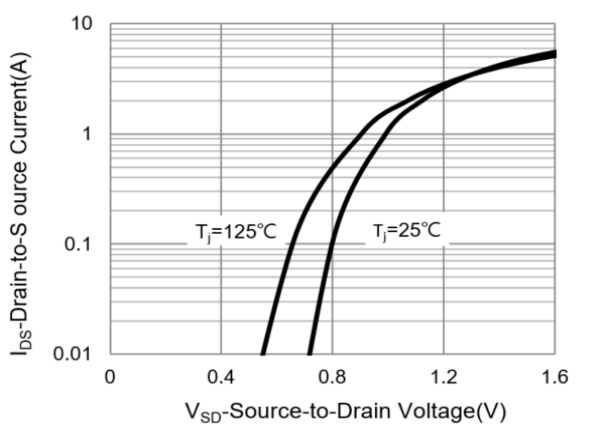

Fig.6 Body Diode Characteristics

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TYPICAL CHARACTERISTIC CURVES

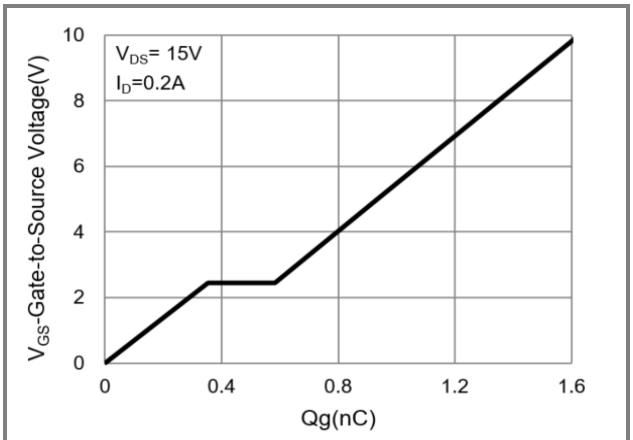


Fig.7 Gate-Charge Characteristics

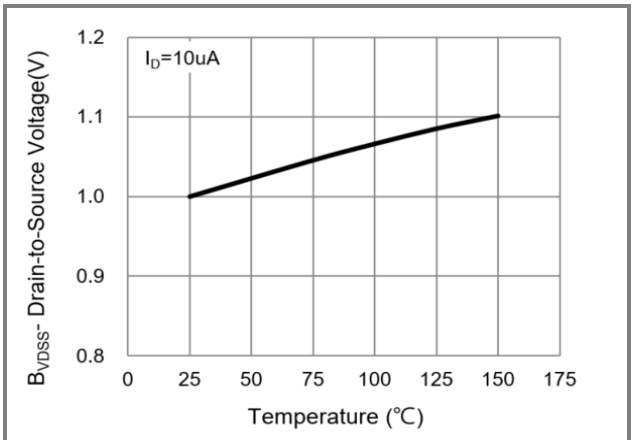


Fig.8 Breakdown Voltage Variation vs. Temperature

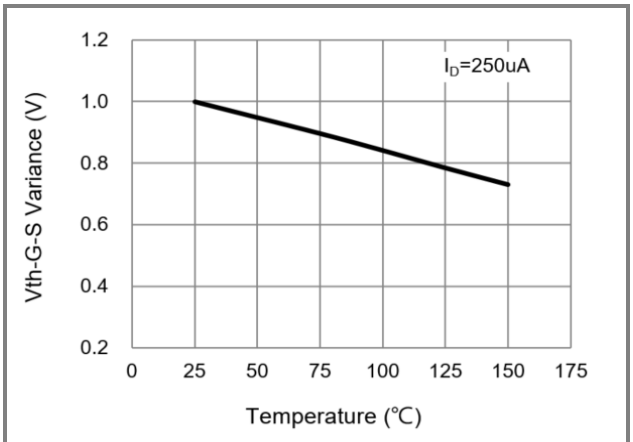


Fig.9 Threshold Voltage Variation with Temperature

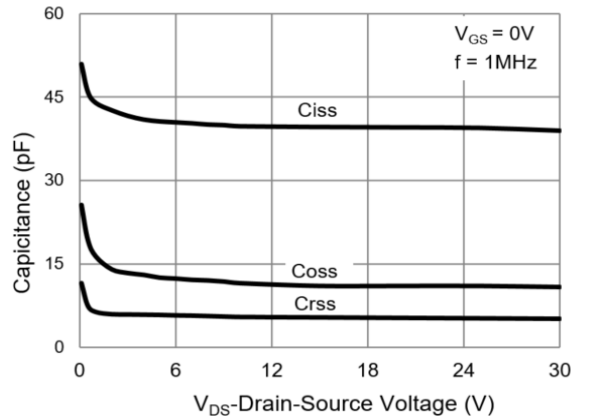


Fig.10 Capacitance vs. Drain-Source Voltage

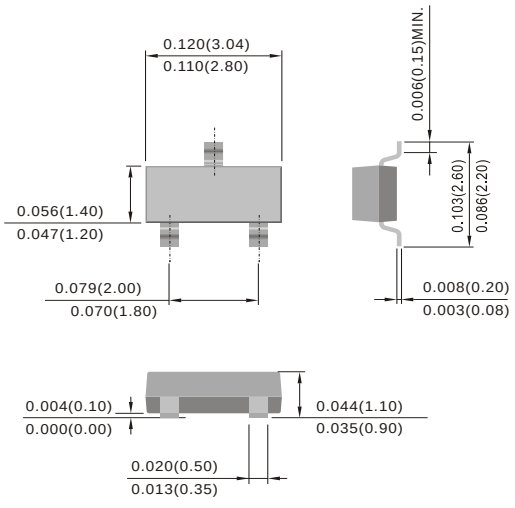
2N7002K

Product and Packing Information

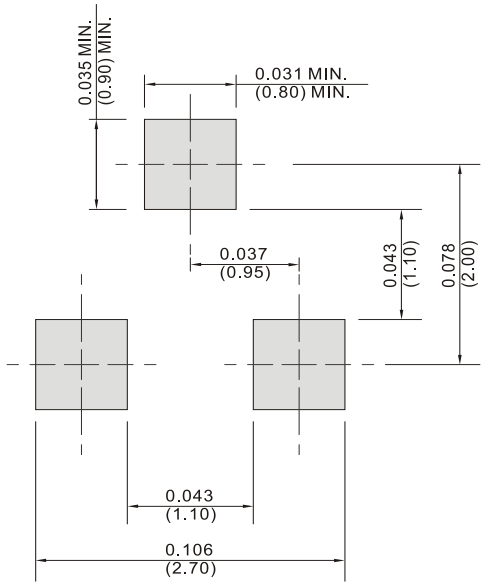
Part No.	Package Type	Packing Type	Marking
2N7002K	SOT-23	3K pcs / 7” reel	K72

Packaging Information & Mounting Pad Layout

SOT-23 Dimension — Unit: inch(mm)



SOT-23 Pad Layout — Unit:1inch(mm)



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