LM5050-1, LM5050-1-Q1 High-Side OR-ing FET Controller

1 Features

- Available in Standard and AEC-Q100 Qualified Versions LM5050Q0MK-1 (up to 150°C T_J) and LM5050Q1MK-1 (up to 125°C T_J)
- Functional safety capable
  - Documentation available to aid functional safety system design
- Wide Operating Input Voltage Range, V_{IN}: 1 V to 75 V (V_{BIAS} required for V_{IN} < 5 V)
- 100-V Transient Capability
- Charge Pump Gate Driver for External N-Channel MOSFET
- Fast 50-ns Response to Current Reversal
- 2-A Peak Gate Turnoff Current
- Minimum V_{DS} Clamp for Faster Turnoff
- Package: SOT-6 (Thin SOT-23-6)

2 Applications

Active OR-ing of Redundant (N+1) Power Supplies

3 Description

The LM5050-1/-Q1 High Side OR-ing FET Controller operates in conjunction with an external MOSFET as an ideal diode rectifier when connected in series with a power source. This ORing controller allows MOSFETs to replace diode rectifiers in power distribution networks thus reducing both power loss and voltage drops.

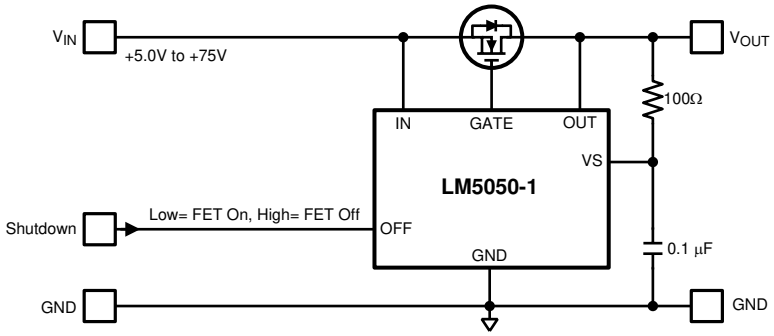
The LM5050-1/-Q1 controller provides charge pump gate drive for an external N-Channel MOSFET and a fast response comparator to turn off the FET when current flows in the reverse direction. The LM5050-1/-Q1 can connect power supplies ranging from 5 V to 75 V and can withstand transients up to 100 V.

Device Information(1)

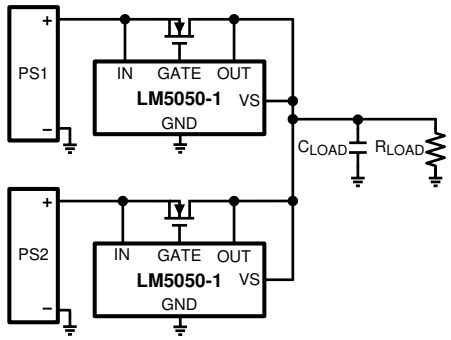
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5050-1	SOT (6)	2.90 mm × 1.60 mm
LM5050-1-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Full Application



Typical Redundant Supply Configuration



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4 Revision History

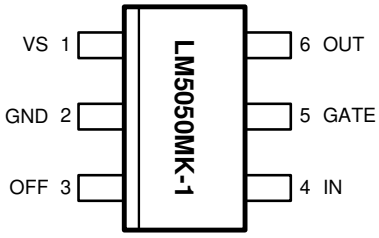
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (December 2015) to Revision F	Page
• Added Functional safety capable link to the *Features* section	1

Changes from Revision D (June 2013) to Revision E	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

DDC Package
6-Pin SOT
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VS	I	The main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump. Typically connected to either V_{OUT} or V_{IN}; a separate supply can also be used.
2	GND	PWR	Ground return for the controller
3	OFF	I	A logic high state at the OFF pin will pull the GATE pin low and turn off the external MOSFET. Note that when the MOSFET is off, current will still conduct through the FET's body diode. This pin should may be left open or connected to GND if unused.
4	IN	I	Voltage sense connection to the external MOSFET Source pin.
5	GATE	O	Connect to the Gate of the external MOSFET. Controls the MOSFET to emulate a low forward-voltage diode.
6	OUT	O	Voltage sense connection to the external MOSFET Drain pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
IN, OUT Pins to Ground(2)	–0.3	100	V
GATE Pin to Ground(2)	–0.3	100	V
VS Pin to Ground	–0.3	100	V
OFF Pin to Ground	–0.3	7	V
Storage Temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The GATE pin voltage is typically 12 V above the IN pin voltage when the LM5050-1 is enabled (that is, OFF Pin is Open or Low, and VIN > VOUT). Therefore, the absolute maximum rating for the IN pin voltage applies only when the LM5050-1 is disabled (that is, OFF Pin is logic high), or for a momentary surge to that voltage because the Absolute Maximum Rating for the GATE pin is also 100 V

6.2 ESD Ratings: LM5050-1

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model (MM)(2)	±150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The MM is a 200-pF capacitor discharged through a 0-Ω resistor (that is, directly) into each pin. Applicable test standard is JESD-A115-A.

6.3 ESD Ratings: LM5050-1-Q1

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Machine model (MM)(2)	±150	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The MM is a 200-pF capacitor discharged through a 0-Ω resistor (that is, directly) into each pin. Applicable test standard is JESD-A115-A.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
IN, OUT, VS Pins		5	75	V
OFF Pin		0	5.5	V
Junction Temperature (T_J)	Standard Grade	−40	125	°C
	LM5050Q0MK-1	−40	150	°C
	LM5050Q1MK-1	−40	125	°C

6.5 Thermal Information

THERMAL METRIC(1)		LM5050-1/-Q1 DDC (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Thermal Information (continued)

THERMAL METRIC[1]		LM5050-1/-Q1 DDC (SOT) 6 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

6.6 Electrical Characteristics

Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12 V, V_{VS} = V_{IN}, V_{OUT} = V_{IN}, V_{OFF} = 0 V, C_{GATE}= 47 nF, and T_J = 25°C.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
VS PIN								
V_{VS}	Operating Supply Voltage Range	T_J = –40°C to 125°C			5		75	V
I_{VS}	Operating Supply Current	V_{VS}= 5 V, V_{IN} = 5 V V_{OUT} = V_{IN} - 100 mV	T_J = 25°C			75		µA
			T_J = –40°C to 125°C				105	
		V_{VS}= 12 V, V_{IN} = 12 V V_{OUT} = V_{IN} - 100 mV	T_J = 25°C			100		
			T_J = –40°C to 125°C				147	
		V_{VS}= 75 V, V_{IN} = 75 V V_{OUT} = V_{IN} - 100 mV	T_J = 25°C			130		
			T_J = –40°C to 125°C				288	
IN PIN								
V_{IN}	Operating Input Voltage Range	T_J = –40°C to 125°C			5		75	V
I_{IN}	IN Pin current	V_{IN} = 5 V V_{VS}= V_{IN} V_{OUT} = V_{IN} - 100 mV GATE = Open	T_J = 25°C			190		µA
			T_J = –40°C to 125°C		32		305	
		V_{IN} = 12 V to 75 V V_{VS}= V_{IN} V_{OUT} = V_{IN} - 100 mV GATE = Open	T_J = 25°C			320		
			T_J = –40°C to 125°C	LM5050MK-1, LM5050Q1MK-1	233		400	
			T_J = –40°C to 125°C	LM5050Q0MK-1	233		475	
OUT PIN								
V_{OUT}	Operating Output Voltage Range	T_J = –40°C to 125°C			5		75	V
I_{OUT}	OUT Pin Current	V_{IN} = 5 V to 75 V V_{VS}= V_{IN} V_{OUT} = V_{IN} - 100 mV	T_J = 25°C			3.2		µA
			T_J = –40°C to 125°C				8	
GATE PIN								
$I_{GATE(ON)}$	Gate Pin Source Current	V_{IN} = 5 V V_{VS} = V_{IN} V_{GATE} = V_{IN} V_{OUT} = V_{IN} - 175 mV	T_J = 25°C			30		µA
			T_J = –40°C to 125°C		12		41	
		V_{IN} = 12 V to 75 V V_{VS} = V_{IN} V_{GATE} = V_{IN} V_{OUT} = V_{IN} - 175 mV	T_J = 25°C			32		
			T_J = –40°C to 125°C		20		41	
V_{GS}	V_{GATE} - V_{IN} in Forward Operation[1]	V_{IN} = 5 V V_{VS} = V_{IN} V_{OUT} = V_{IN} - 175 mV	T_J = 25°C			7		V
			T_J = –40°C to 125°C		4		9	
		V_{IN} = 12 V to 75 V V_{VS} = V_{IN} V_{OUT} = V_{IN} - 175 mV	T_J = 25°C			12		
			T_J = –40°C to 125°C		9		14	

(1) Measurement of V_{GS} voltage (that is. V_{GATE} - V_{IN}) includes 1 MΩ in parallel with C_{GATE}.

Electrical Characteristics (continued)

Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12 V, V_{VS} = V_{IN}, V_{OUT} = V_{IN}, V_{OFF} = 0 V, C_{GATE}= 47 nF, and T_J = 25°C.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{GATE(REV)}$	Gate Capacitance Discharge Time at Forward to Reverse Transition See Figure 1	C_{GATE} = 0 (2)	T_J = 25°C			25		ns
			T_J = –40°C to 125°C				85	
		C_{GATE} = 10 nF (2)	T_J = 25°C			60		
		C_{GATE} = 47 nF (2)	T_J = 25°C			180		
			T_J = –40°C to 125°C				350	
$t_{GATE(OFF)}$	Gate Capacitance DischargeTime at OFF pin Low to High Transition See Figure 2	C_{GATE} = 47 nF (3)	T_J = 25°C			486		ns
$I_{GATE(OFF)}$	Gate Pin Sink Current	V_{GATE} = V_{IN} + 3 V V_{OUT} > V_{IN} + 100 mV t ≤ 10 ms	T_J = 25°C			2.8		A
			T_J = –40°C to 125°C	LM5050MK-1, LM5050Q1MK-1	1.8			
			T_J = –40°C to 125°C	LM5050Q0MK-1	1.4			
$V_{SD(REV)}$	Reverse V_{SD} Threshold V_{IN} < V_{OUT}	V_{IN} - V_{OUT}	T_J = 25°C			–28		mV
			T_J = –40°C to 125°C		–41		–16	
$\Delta V_{SD(REV)}$	Reverse V_{SD} Hysteresis		T_J = 25°C			10		mV
$V_{SD(REG)}$	Regulated Forward V_{SD} Threshold V_{IN} > V_{OUT}	V_{IN} = 5 V V_{VS} = V_{IN} V_{IN} - V_{OUT}	T_J = 25°C			19		mV
			T_J = –40°C to 125°C	LM5050MK-1, LM5050Q1MK-1	1		37	
			T_J = –40°C to 125°C	LM5050Q0MK-1	1		60	
			T_J = 25°C			22		
		V_{IN} = 12 V V_{VS} = V_{IN} V_{IN} - V_{OUT}	T_J = –40°C to 125°C	LM5050MK-1, LM5050Q1MK-1	4.4		37	
			T_J = –40°C to 125°C	LM5050Q0MK-1	4.4		60	
OFF PIN								
$V_{OFF(IH)}$	OFF Input High Threshold Voltage	V_{OUT} = V_{IN}-500 mV V_{OFF} Rising	T_J = 25°C			1.56		V
			T_J = –40°C to 125°C				1.75	
$V_{OFF(IL)}$	OFF Input Low Threshold Voltage	V_{OUT} = V_{IN} - 500 mV V_{OFF} Falling	T_J = 25°C			1.4		
			T_J = –40°C to 125°C		1.1			
ΔV_{OFF}	OFF Threshold Voltage Hysteresis	$V_{OFF(IH)}$ - $V_{OFF(IL)}$	T_J = 25°C			155		mV
I_{OFF}	OFF Pin Internal Pulldown	V_{OFF} = 4.5 V	T_J = 25°C			5		µA
			T_J = –40°C to 125°C		3		7	
		V_{OFF} = 5 V	T_J = 25°C			8		

(2) Time from V_{IN}-V_{OUT} voltage transition from 200 mV to -500 mV until GATE pin voltage falls to V_{IN} + 1 V. See Figure 1.
(3) Time from V_{OFF} voltage transition from 0 V to 5 V until GATE pin voltage falls to V_{IN} + 1 V. See Figure 2

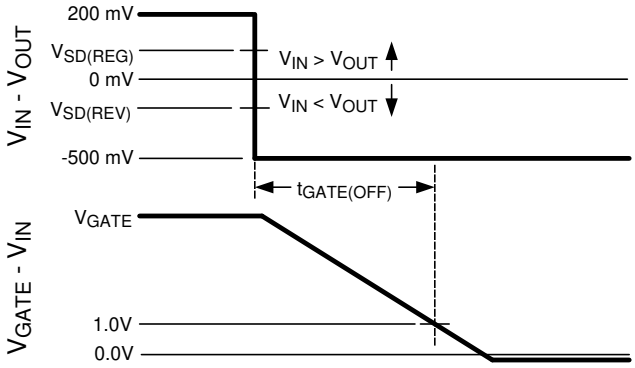


Figure 1. Gate OFF Timing for Forward to Reverse Transition

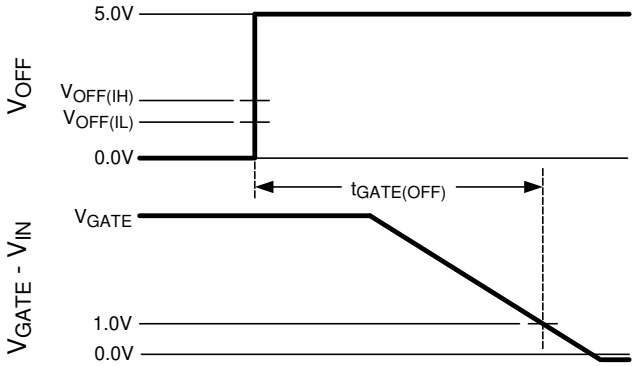


Figure 2. Gate OFF Timing for OFF Pin Low to High Transition

6.7 Typical Characteristics

Unless otherwise stated: V_{VS} = 12 V, V_{IN} = 12 V, V_{OFF} = 0 V, and T_J = 25°C

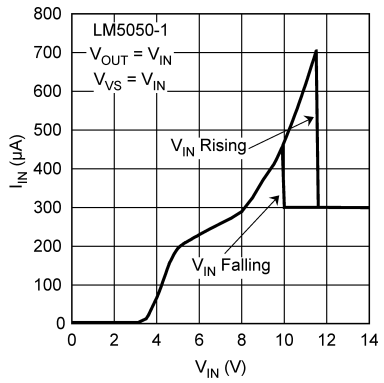


Figure 3. I_{IN} vs V_{IN}

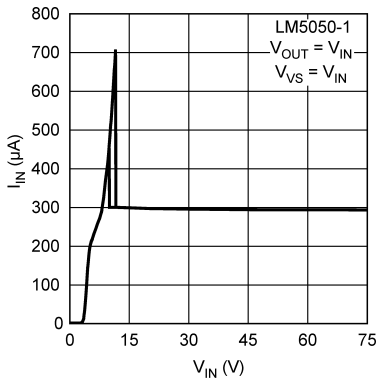


Figure 4. I_{IN} vs V_{IN}

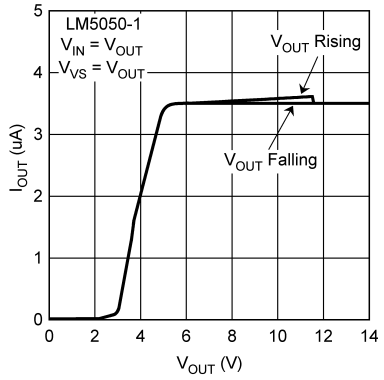


Figure 5. I_{OUT} vs V_{OUT}

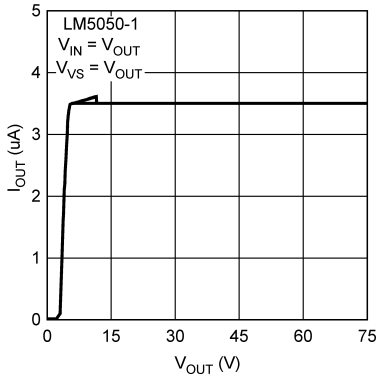


Figure 6. I_{OUT} vs V_{OUT}

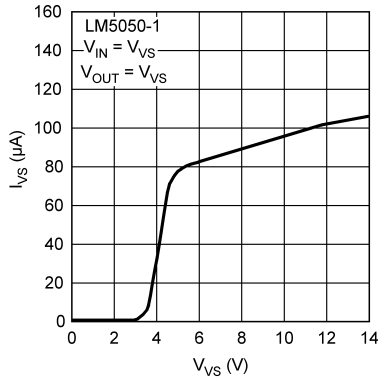


Figure 7. I_{VS} vs V_{VS}

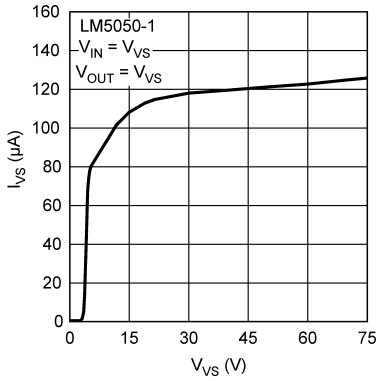


Figure 8. I_{VS} vs V_{VS}

Typical Characteristics (continued)

Unless otherwise stated: V_{VS} = 12 V, V_{IN} = 12 V, V_{OFF} = 0 V, and T_J = 25°C

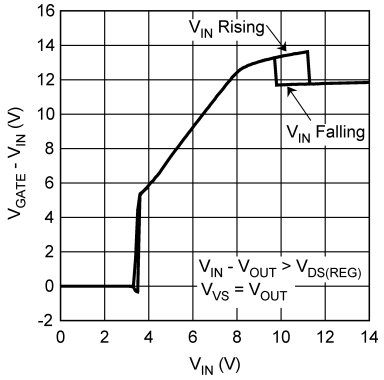


Figure 9. (V_{GATE} - V_{IN}) vs V_{IN}, V_{VS} = V_{OUT}

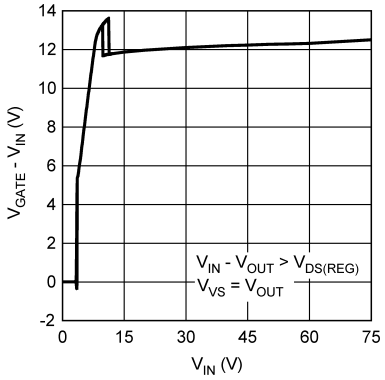


Figure 10. (V_{GATE} - V_{IN}) vs V_{IN}, V_{VS} = V_{OUT}

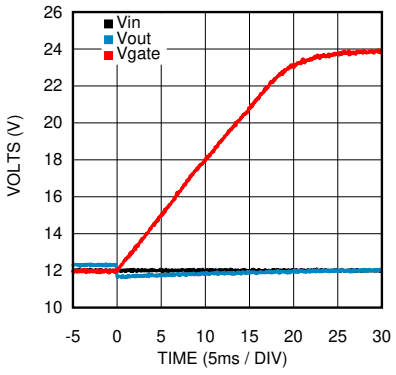


Figure 11. Forward C_{GATE} Charge Time, C_{GATE} = 47 nF

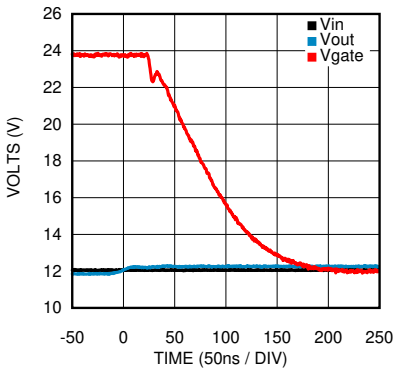


Figure 12. Reverse C_{GATE} Discharge, C_{GATE} = 47 nF

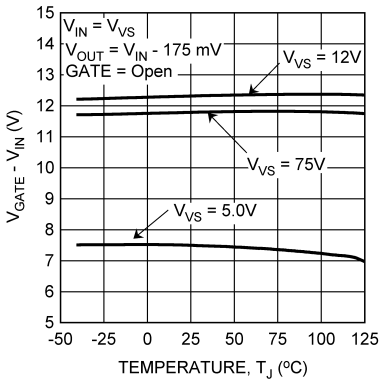


Figure 13. V_{GATE} - V_{IN} vs Temperature

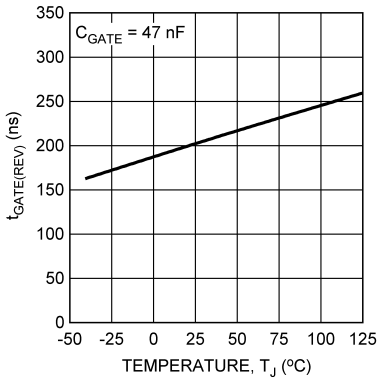


Figure 14. $t_{GATE(REV)}$ vs Temperature

Typical Characteristics (continued)

Unless otherwise stated: V_{VS} = 12 V, V_{IN} = 12 V, V_{OFF} = 0 V, and T_J = 25°C

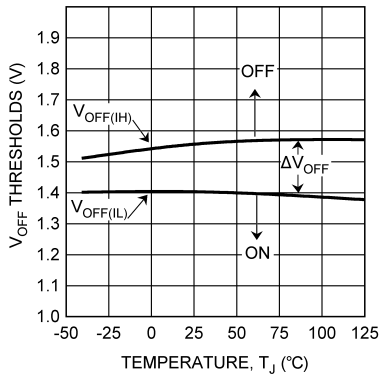


Figure 15. OFF Pin Thresholds vs Temperature

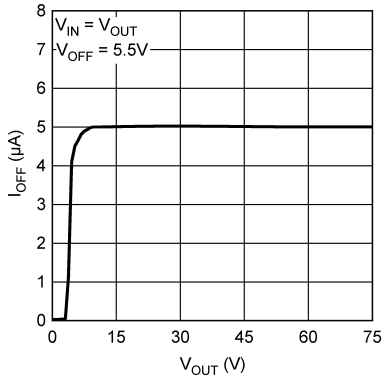


Figure 16. OFF Pin Pulldown vs Temperature

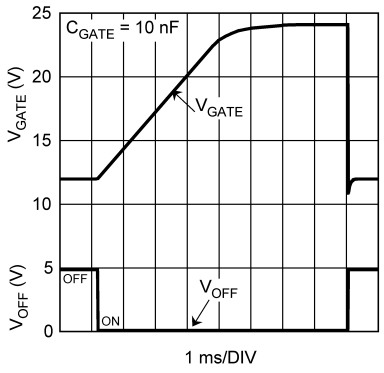


Figure 17. C_{GATE} Charge and Discharge vs OFF Pin

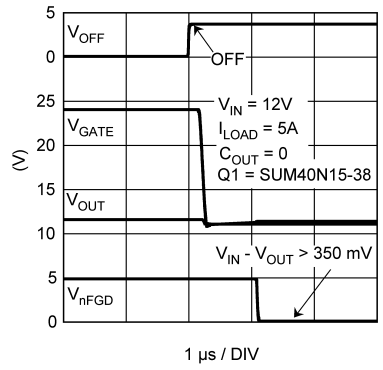


Figure 18. OFF Pin, ON to OFF Transition

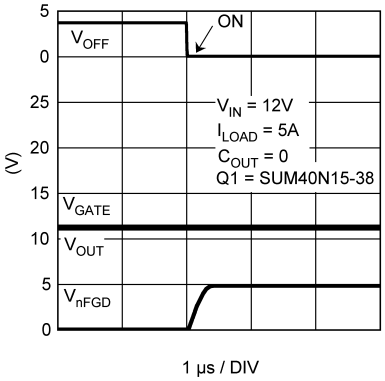


Figure 19. OFF Pin, OFF to ON Transition

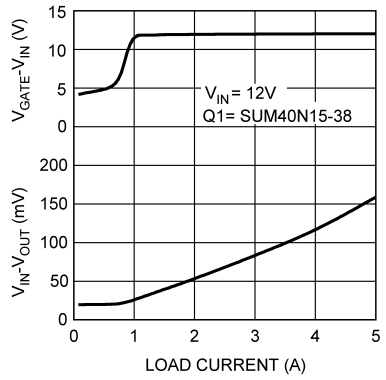


Figure 20. GATE Pin vs ($R_{DS(ON)}$ × I_{DS})

7 Detailed Description

7.1 Overview

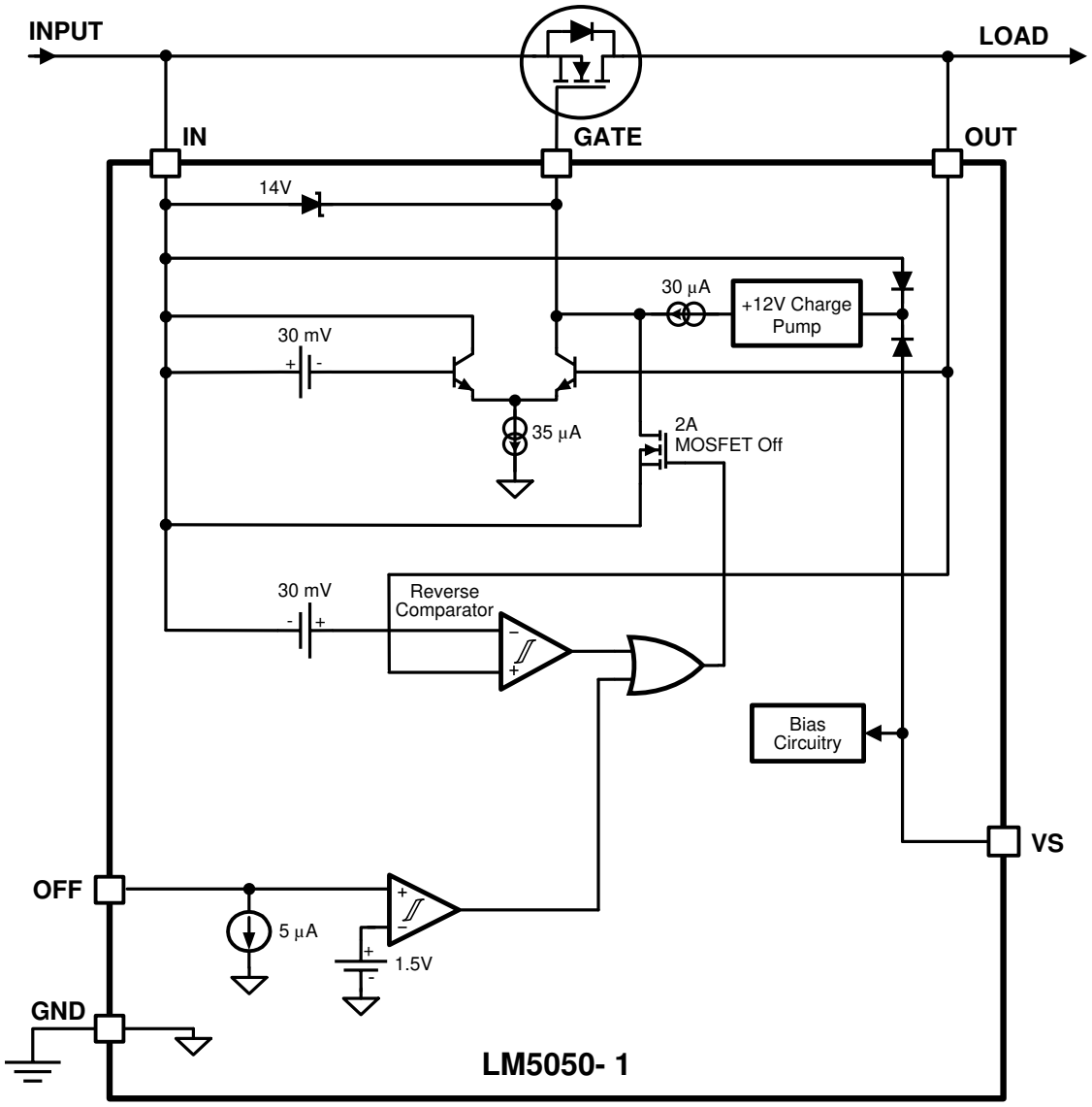
Blocking diodes are commonly placed in series with supply inputs for the purpose of ORing redundant power sources and protecting against supply reversal. The LM5050 replaces diodes in these applications with an N-MOSFET to reduce both the voltage drop and power loss associated with a passive solution. At low input voltages, the improvement in forward voltage loss is readily appreciated where headroom is tight, as shown in Figure 2. The LM5050 operates from 5 V to 75 V and it can withstand an absolute maximum of 100 V without damage. A 12-V or 15-A ideal diode application is shown in Figure 24. Several external components are included in addition to the MOSFET, Q1. Ideal diodes, like their non-ideal counterparts, exhibit a behavior known as reverse recovery. In combination with parasitic or intentionally introduced inductances, reverse recovery spikes may be generated by an ideal diode during an reverse current shutdown. D1, D2 and R1 protect against these spikes which might otherwise exceed the LM5050 100-V survival rating. COUT also plays a role in absorbing reverse recovery energy. Spikes and protection schemes are discussed in detail in the *Short Circuit Failure of an Input Supply* section.

NOTE

The OFF pin may be used to active the GATE pull down circuit and turn off the pass MOSFET, but it does not disconnect the load from the input because Q1's body diode is still present.

If Vs is powered while IN is floating or grounded, then about 0.5mA will leak from the Vs pin into the IC and about 3mA will leak from the OUT pin into the IC. From this leakage, about 50 uA will flow out of the IN pin and the rest will flow to ground. This does not affect long term reliability of the IC, but may influence circuit design. See *Reverse Input Voltage Protection With IQ Reduction* for details on how to avoid this leakage current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IN, GATE, and OUT Pins

When power is initially applied, the load current will flow from source to drain through the body diode of the MOSFET. Once the voltage across the body diode exceeds $V_{SD(REG)}$ then the LM5050-1 begins charging the MOSFET gate through a 32 µA (typical) charge pump current source . In forward operation, the gate of the MOSFET is charged until it reaches the clamping voltage of the 12-V GATE to IN pin Zener diode internal to the LM5050-1.

The LM5050-1 is designed to regulate the MOSFET gate-to-source voltage. If the MOSFET current decreases to the point that the voltage across the MOSFET falls below the $V_{SD(REG)}$ voltage regulation point of 22 mV (typical), the GATE pin voltage will be decreased until the voltage across the MOSFET is regulated at 22 mV. If the source-to-drain voltage is greater than the $V_{SD(REG)}$ voltage, the gate-to-source voltage will increase and eventually reach the 12-V GATE to IN pin Zener clamp level.

Feature Description (continued)

If the MOSFET current reverses, possibly due to failure of the input supply, such that the voltage across the LM5050-1 IN and OUT pins is more negative than the $V_{SD(REV)}$ voltage of -28 mV (typical), the LM5050-1 will quickly discharge the MOSFET gate through a strong GATE to IN pin discharge transistor.

If the input supply fails abruptly, as would occur if the supply was shorted directly to ground, a reverse current will temporarily flow through the MOSFET until the gate can be fully discharged. This reverse current is sourced from the load capacitance and from the parallel connected supplies. The LM5050-1 responds to a voltage reversal condition typically within 25 ns. The actual time required to turn off the MOSFET will depend on the charge held by the gate capacitance of the MOSFET being used. A MOSFET with 47 nF of effective gate capacitance can be turned off in typically 180 ns. This fast turnoff time minimizes voltage disturbances at the output, as well as the current transients from the redundant supplies.

7.3.2 VS Pin

The LM5050-1 VS pin is the main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump.

For typical LM5050-1 applications, where the input voltage is above 5 V, the VS pin can be connected directly to the OUT pin. In situations where the input voltage is close to, but not less than, the 5 V minimum, it may be helpful to connect the VS pin to the OUT pin through an RC Low-Pass filter to reduce the possibility of erratic behavior due to spurious voltage spikes that may appear on the OUT and IN pins. The series resistor value should be low enough to keep the VS voltage drop at a minimum. A typical series resistor value is 100 Ω. The capacitor value should be the lowest value that produces acceptable filtering of the voltage noise.

If Vs is powered while IN is floating or grounded, then about 0.5 mA will leak from the Vs pin into the IC and about 3mA will leak from the OUT pin into the IC. From this leakage, about 50 uA will flow out of the IN pin and the rest will flow to ground. This does not affect long term reliability of the IC, but may influence circuit design. See *Reverse Input Voltage Protection With IQ Reduction* for details on how to avoid this leakage current.

Alternately, it is possible to operate the LM5050-1 with V_{IN} value as low as 1 V if the VS pin is powered from a separate supply. This separate VS supply must be from 5 V and 75 V. See Figure 27.

7.3.3 OFF Pin

The OFF pin is a logic level input pin that is used to control the gate drive to the external MOSFET. The maximum operating voltage on this pin is 5.5 V.

When the OFF pin is high, the MOSFET is turned off (independent of the sensed IN and OUT voltages). In this mode, load current will flow through the body diode of the MOSFET. The voltage difference between the IN pin and OUT pins will be approximately 700 mV if the MOSFET is operating normally through the body diode.

The OFF pin has an internal pulldown of 5 µA (typical). If the OFF function is not required the pin may be left open or connected to ground.

7.4 Device Functional Modes

7.4.1 ON/OFF Control Mode

The MOSFET can be turned off by asserting the OFF pin high. This mode only disables the MOSFET, but V_{OUT} is still available through the body diode of the MOSFET.

7.4.2 External Power Supply Mode

The Vs pin of the LM5050 can be operated from 5 V to 75 V as the bias input supply. In this mode V_{IN} voltage can be as low as 1 V, as shown in Figure 27.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Systems that require high availability often use multiple, parallel-connected redundant power supplies to improve reliability. Schottky OR-ing diodes are typically used to connect these redundant power supplies to a common point at the load. The disadvantage of using OR-ing diodes is the forward voltage drop, which reduces the available voltage and the associated power losses as load currents increase. Using an N-channel MOSFET to replace the OR-ing diode requires a small increase in the level of complexity, but reduces, or eliminates, the need for diode heat sinks or large thermal copper area in circuit board layouts for high power applications.

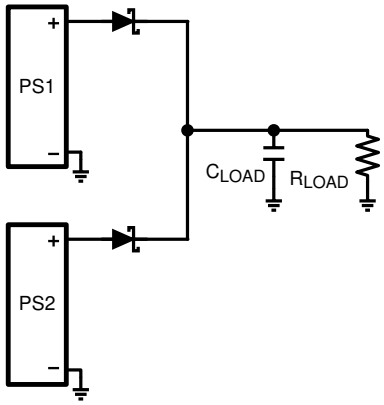


Figure 21. OR-ing with Diodes

The LM5050-1/-Q1 is a positive voltage (that is, high-side) OR-ing controller that will drive an external N-channel MOSFET to replace an OR-ing diode. The voltage across the MOSFET source and drain pins is monitored by the LM5050-1 at the IN and OUT pins, while the GATE pin drives the MOSFET to control its operation based on the monitored source-drain voltage. The resulting behavior is that of an ideal rectifier with source and drain pins of the MOSFET acting as the anode and cathode pins of a diode respectively.

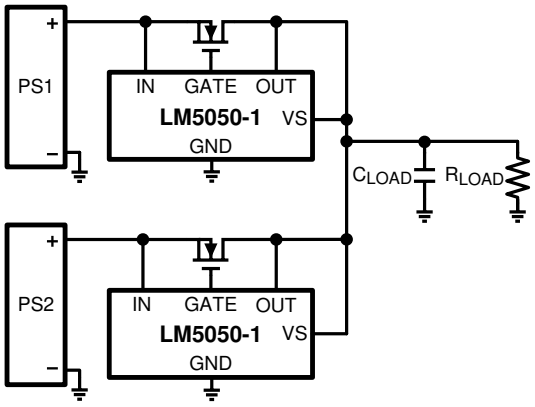


Figure 22. OR-ing With MOSFETs

Application Information (continued)

8.1.1 MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous Drain current I_D, the maximum Source current (that is, body diode) I_S, the maximum drain-to-source voltage $V_{DS(MAX)}$, the gate-to-source threshold voltage $V_{GS(TH)}$, the drain-to-source reverse breakdown voltage $V_{(BR)DSS}$, and the drain-to-source On resistance $R_{DS(ON)}$.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The rating for the maximum current through the body diode, I_S, is typically rated the same as, or slightly higher than the drain current, but body diode current only flows while the MOSFET gate is being charged to $V_{GS(TH)}$.

Gate Charge Time = Q_g / $I_{GATE(ON)}$

1. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions.
2. The drain-to-source reverse breakdown voltage, $V_{(BR)DSS}$, may provide some transient protection to the OUT pin in low voltage applications by allowing conduction back to the IN pin during positive transients at the OUT pin.
3. The gate-to-source threshold voltage, $V_{GS(TH)}$, should be compatible with the LM5050-1 gate drive capabilities. Logic level MOSFETs, with $R_{DS(ON)}$ rated at $V_{GS(TH)}$ at 5 V, are recommended, but sub-Logic level MOSFETs having $R_{DS(ON)}$ rated at $V_{GS(TH)}$ at 2.5 V, can also be used.
4. The dominate MOSFET loss for the LM5050-1 active OR-ing controller is conduction loss due to source-to-drain current to the output load, and the $R_{DS(ON)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(ON)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(ON)}$ may not always give desirable results for several reasons:
    1. Reverse transition detection. Higher $R_{DS(ON)}$ will provide increased voltage information to the LM5050-1 Reverse Comparator at a lower reverse current level. This will give an earlier MOSFET turnoff condition should the input voltage become shorted to ground. This will minimize any disturbance of the redundant bus.
    2. Reverse current leakage. In cases where multiple input supplies are closely matched it may be possible for some small current to flow continuously through the MOSFET drain to source (that is, reverse) without activating the LM5050-1 Reverse Comparator. Higher $R_{DS(ON)}$ will reduce this reverse current level.
    3. Cost. Generally, as the $R_{DS(ON)}$ rating goes lower, the cost of the MOSFET goes higher.
5. The dominate MOSFET loss for the LM5050-1 active OR-ing controller is conduction loss due to source-to-drain current to the output load, and the $R_{DS(ON)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(ON)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(ON)}$ may not always give desirable results for several reasons:
    a. Selecting a MOSFET with an $R_{DS(ON)}$ that is too large will result in excessive power dissipation. Additionally, the MOSFET gate will be charged to the full value that the LM5050-1 can provide as it attempts to drive the Drain to Source voltage down to the $V_{SD(REG)}$ of 22 mV typical. This increased Gate charge will require some finite amount of additional discharge time when the MOSFET needs to be turned off.
    b. As a guideline, it is suggest that $R_{DS(ON)}$ be selected to provide at least 22 mV, and no more than 100 mV, at the nominal load current.
    c. (22 mV / I_D) ≤ $R_{DS(ON)}$ ≤ (100 mV / I_D)
    d. The thermal resistance of the MOSFET package should also be considered against the anticipated dissipation in the MOSFET to ensure that the junction temperature (T_J) is reasonably well controlled, because the $R_{DS(ON)}$ of the MOSFET increases as the junction temperature increases.
6. $P_{DISS} = I_D^2 \times (R_{DS(ON)})$
7. Operating with a maximum ambient temperature ($T_{A(MAX)}$) of 35°C, a load current of 10 A, and an $R_{DS(ON)}$ of 10 mΩ, and desiring to keep the junction temperature under 100°C, the maximum junction-to-ambient thermal resistance rating (θ_{JA}) must be:
    a. $R_{\theta JA} \le (T_{J(MAX)} - T_{A(MAX)})/(I_D^2 \times R_{DS(ON)})$
    b. $R_{\theta JA} \le (100°C - 35°C)/(10\ A \times 10\ A \times 0.01\ \Omega)$

Application Information (continued)

c. $R_{\theta JA} \leq 65°C/W$

8.1.2 Short Circuit Failure of an Input Supply

An abrupt 0-Ω short circuit across the input supply will cause the highest possible reverse current to flow while the internal LM5050-1 control circuitry discharges the gate of the MOSFET. During this time, the reverse current is limited only by the $R_{DS(ON)}$ of the MOSFET, along with parasitic wiring resistances and inductances. Worst case instantaneous reverse current would be limited to:

$$I_{D(REV)} = (V_{OUT} - V_{IN}) / R_{DS(ON)} \quad (1)$$

The internal Reverse Comparator will react, and will start the process of discharging the Gate, when the reverse current reaches:

$$I_{D(REV)} = V_{SD(REV)} / R_{DS(ON)} \quad (2)$$

When the MOSFET is finally switched off, the energy stored in the parasitic wiring inductances will be transferred to the rest of the circuit. As a result, the LM5050-1 IN pin will see a negative voltage spike while the OUT pin will see a positive voltage spike. The IN pin can be protected by diode clamping the pin to GND in the negative direction. The OUT pin can be protected with a TVS protection diode, a local bypass capacitor, or both. In low voltage applications, the MOSFET drainto- source breakdown voltage rating may be adequate to protect the OUT pin (that is, $V_{IN} + V_{(BR)DSS(MAX)} < 75$ V), but most MOSFET data sheets do not ensure the maximum breakdown rating, so this method should be used with caution.

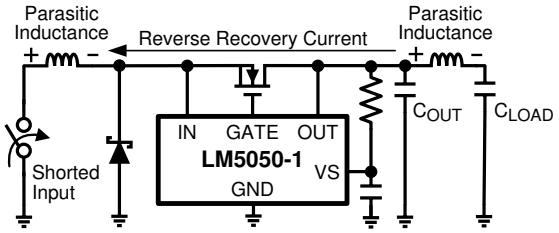


Figure 23. Reverse Recovery Current Generates Inductive Spikes at VIN and VOUT pins.

8.2 Typical Applications

8.2.1 Typical Application With Input and Output Transient Protection

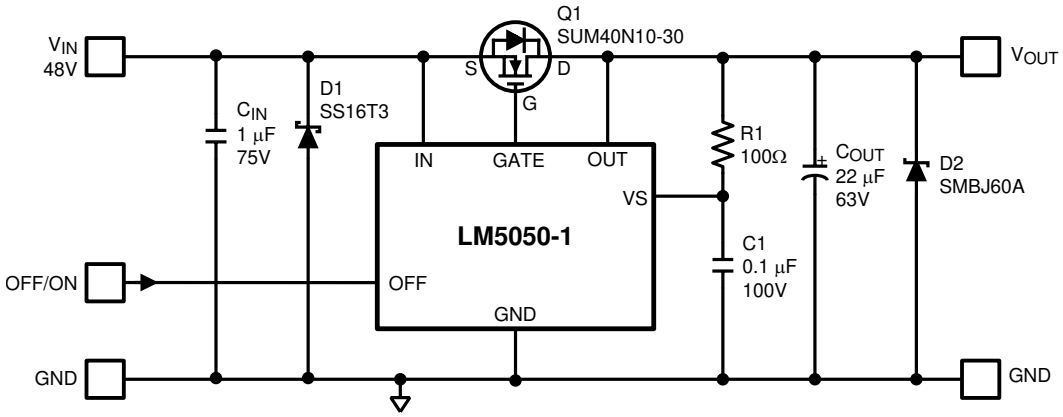


Figure 24. Typical Application With Input and Output Transient Protection Schematic

Typical Applications (continued)

8.2.1.1 Design Requirements

Table 1 shows the parameters for Figure 24

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum Input Voltage, VIN_{MIN}	6 V
Maximum Input Voltage, VIN_{Max}	50 V
Output Current Range, IOUT	0 to 15 A
Ambient Temperature Range, T_A	0°C to 50°C

8.2.1.2 Detailed Design Procedure

The following design procedure can be used to select component values for the LM5050-1.

8.2.1.2.1 Power Supply Components (R1 C1,) Selection

The LM5050-1 VS pin is the main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump. The series resistor (R1) value should be low enough to keep the VS voltage drop at a minimum. A typical series resistor value is 100 Ω. The capacitor value (0.1 uF typical) should be the lowest value that produces acceptable filtering of the voltage noise.

8.2.1.2.2 MOSFET (Q1) Selection

The MOSFET (Q1) selection procedure is explained in detail in *MOSFET Selection*. The MOSFET used in the design example is SUM40N10-30-E3.

8.2.1.2.3 D1 and D2 Selection for Inductive Kick-Back Protection

Diode D1 and capacitor C1 and diode D2 and capacitor C2 in the Figure 27 serve as inductive kick-back protection to limit negative transient voltage spikes generated on the input when the input supply voltage is abruptly shorted to zero volts. As a result, the LM5050-1 IN pin will see a negative voltage spike while the OUT pin will see a positive voltage spike. The IN pin can be protected by schottky diode (D1) clamping the pin to GND in the negative direction, similarly the OUT pin should be protected with a TVS protection diode (D1), or with a local bypass capacitor, or both. D1 is selected as 1-A, 60-V Schottky Barrier Rectifier (SS16T3G) and D2 is the 60 V, TVS (SMBJ60A-13-F).

8.2.1.3 Application Curves

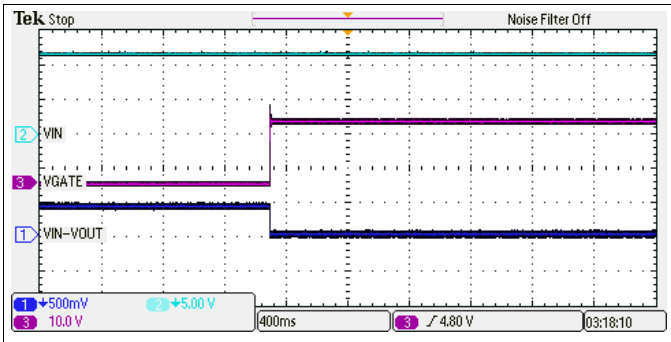


Figure 25. Forward voltage (VIN-VOUT) Drop Reduces When Gate is Enabled (VIN = 12 V)

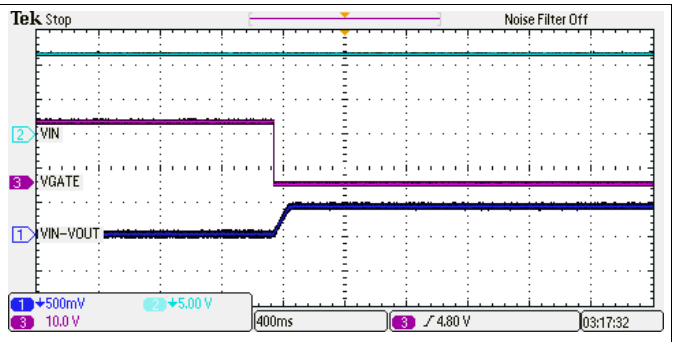


Figure 26. Forward Voltage (VIN-VOUT) Drop Increases When Gate is Disabled (VIN = 12 V)

8.2.2 Using a Separate VS Supply for Low Vin Operation

In some applications, it is desired to operate LM5050-1 from low supply voltage. The LM5050-1 can operate with a 1-V rail voltage, provided its VS pin is biased from 5 V to 75 V. The detail of such application is depicted in Figure 27.

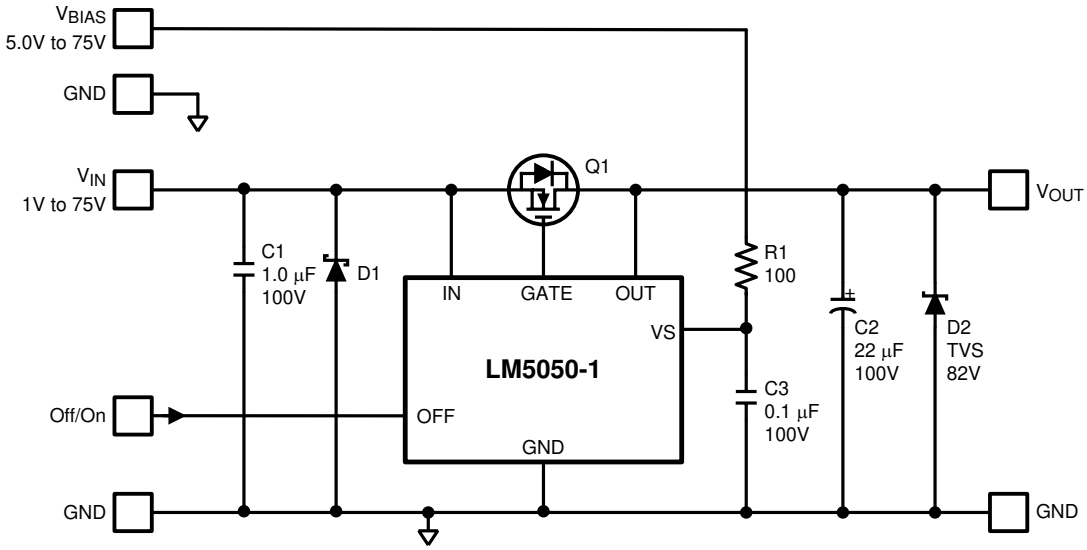


Figure 27. Using a Separate vs Supply for Low Vin Operation Schematic

8.2.3 ORing of Two Power Sources

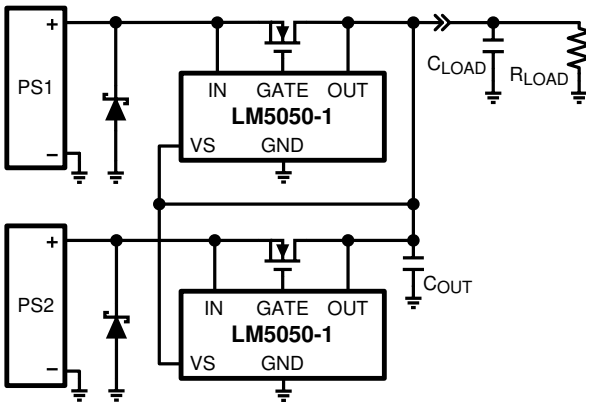


Figure 28. ORing of Two Power Sources

8.2.4 Reverse Input Voltage Protection With IQ Reduction

If Vs is powered while IN is floating or grounded, then about 0.5 mA will leak from the Vs pin into the IC and about 3 mA will leak from the OUT pin into the IC. From this leakage, about 50 uA will flow out of the IN pin and the rest will flow to ground. This does not affect long term reliability of the IC, but may influence circuit design.

In battery powered applications, whenever LM5050-1 functionality is not needed, the supply to the LM5050-1 can be disconnected by turning “OFF” Q2, as shown in Figure 29. This disconnects the ground path of the LM5050-1 and eliminates the current leakage from the battery.

The quiescent current of LM5050-1 can be also reduced by disconnecting the supply to VS pin, whenever LM5050-1 function is not need.

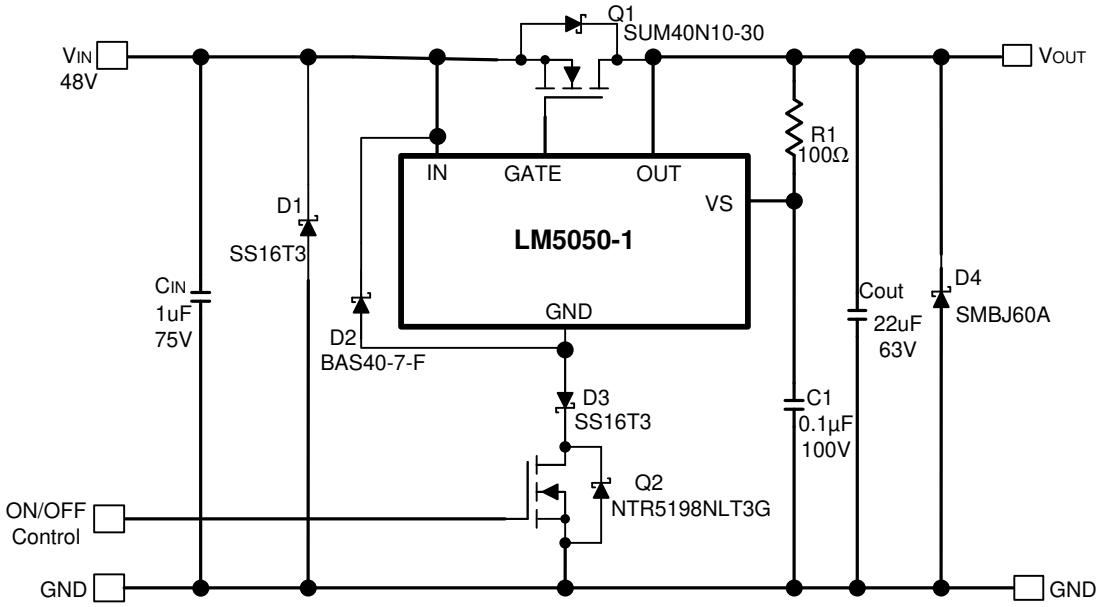


Figure 29. Reverse Input Voltage Protection With IQ Reduction Schematic

8.2.5 Basic Application With Input Transient Protection

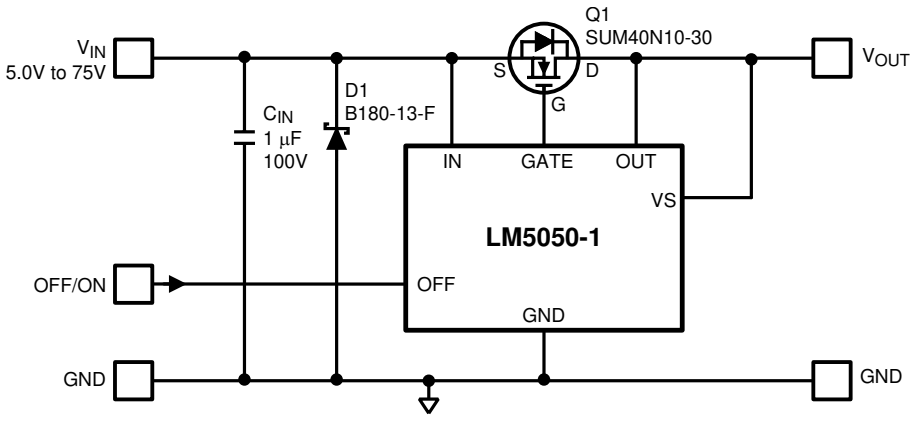


Figure 30. Basic Application With Input Transient Protection Schematic

8.2.6 48-V Application With Reverse Input Voltage (V_{IN} = –48 V) Protection

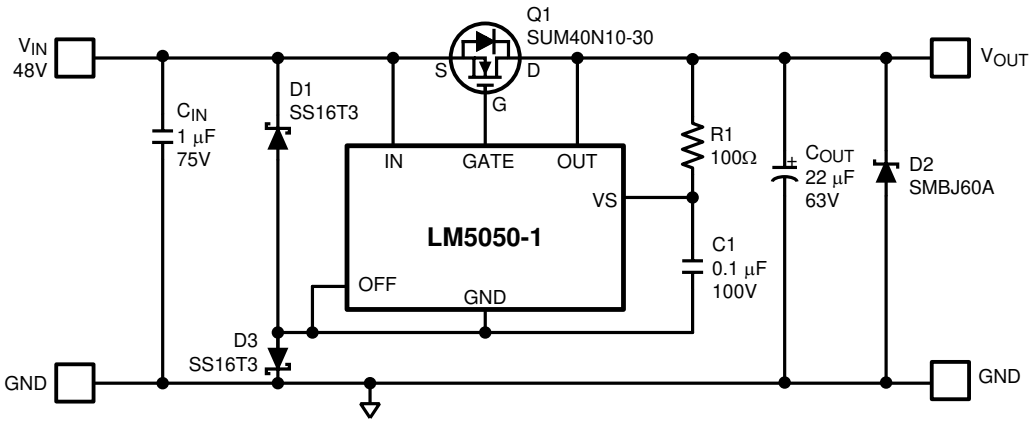


Figure 31. 48-V Application With Reverse Input Voltage (V_{IN} = –48 V) Protection Schematic

8.2.6.1 Application Curves

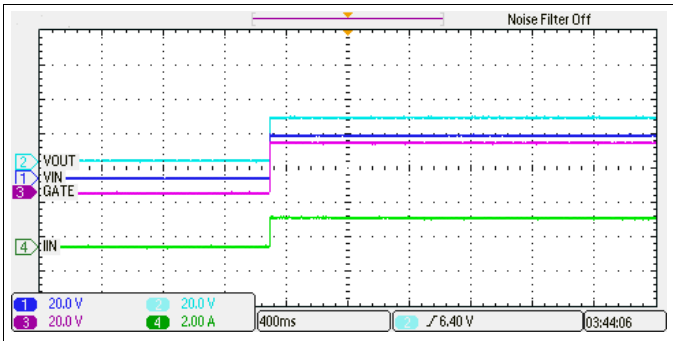


Figure 32. Operation With Positive Polarity Input With (VIN = 25 V)

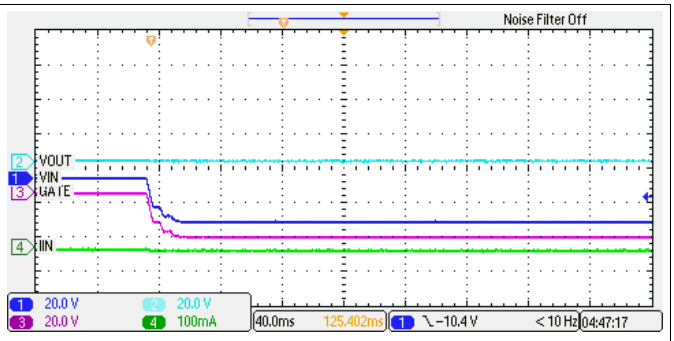


Figure 33. Operation With Negative polarity Input With (VIN = –25 V)

9 Power Supply Recommendations

When the LM5050-1/-Q1 shuts off the external MOSFET, transient voltages will appear on the input and output due to reverse recovery, as discussed in *Short Circuit Failure of an Input Supply*.To prevent LM5050-1 and surrounding components from damage under the conditions of a direct input short circuit, it is necessary to clamp the negative transient at IN, and OUT pins with TVS.

10 Layout

10.1 Layout Guidelines

The typical PCB layout for LM5050-1/-Q1 is shown in Figure 34. TI recommends connecting the IN, Gate and OUT pins close to the source and drain pins of the MOSFET. Keep the traces of the MOSFET drain wide and short to minimize resistive losses. Place surge suppressors (D1 and D4) components as shown in the example layout of LM5050-1 in *Layout Example*.

10.2 Layout Example

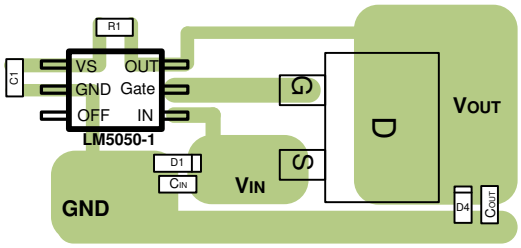


Figure 34. Typical Layout Example With D2PAK N-MOSFET

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

Achieving Stable VGS Using LM5050-1 with Low Current and Noisy Input Supply, SLVA684

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM5050-1	Click here	Click here	Click here	Click here	Click here
LM5050-1-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5050MK-1/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SZHB	Samples
LM5050MKX-1/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SZHB	Samples
LM5050Q0MK-1/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 150	SL5B	Samples
LM5050Q0MKX-1/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 150	SL5B	Samples
LM5050Q1MK-1/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SP3B	Samples
LM5050Q1MKX-1/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SP3B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM5050-1, LM5050-1-Q1 :

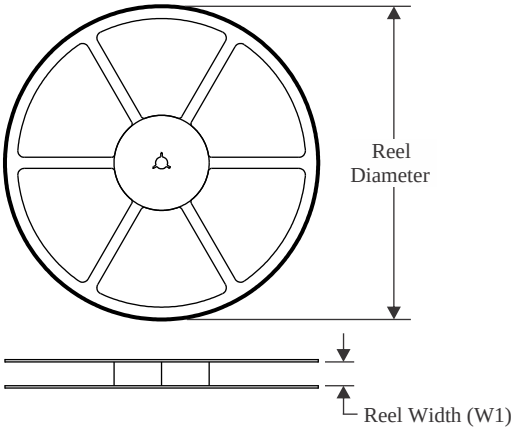
- Catalog: LM5050-1
- Automotive: LM5050-1-Q1

NOTE: Qualified Version Definitions:

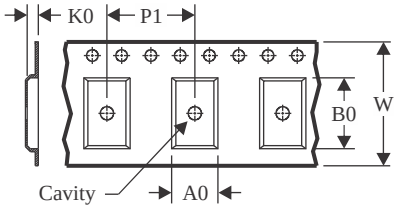
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

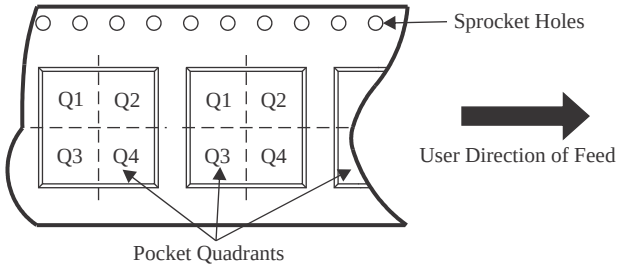


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

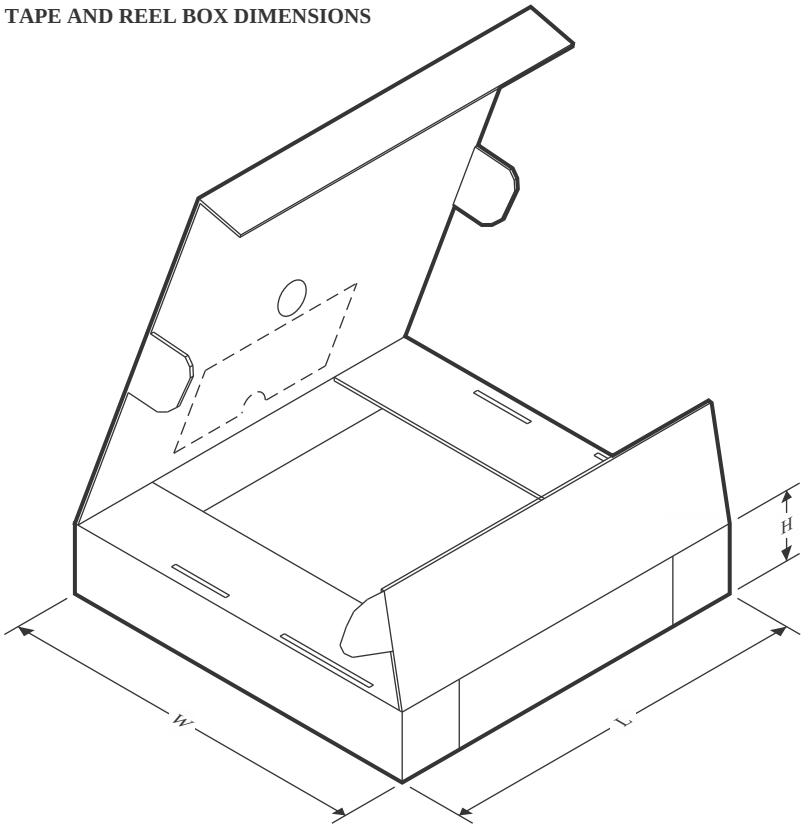
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5050MK-1/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5050MKX-1/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5050Q0MK-1/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5050Q0MKX-1/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5050Q1MK-1/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5050Q1MKX-1/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

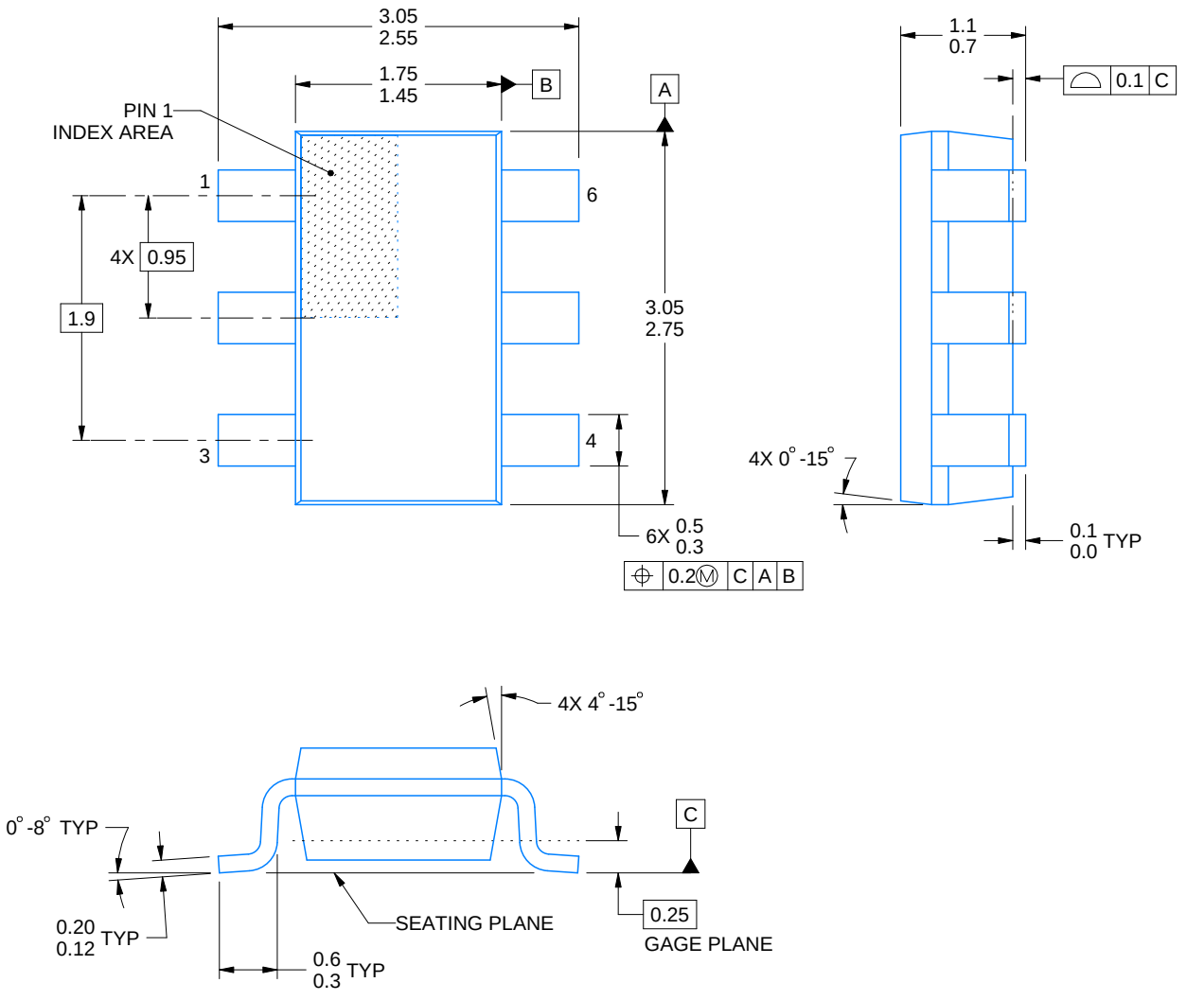
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5050MK-1/NOPB	SOT-23-THIN	DDC	6	1000	208.0	191.0	35.0
LM5050MKX-1/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LM5050Q0MK-1/NOPB	SOT-23-THIN	DDC	6	1000	208.0	191.0	35.0
LM5050Q0MKX-1/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LM5050Q1MK-1/NOPB	SOT-23-THIN	DDC	6	1000	208.0	191.0	35.0
LM5050Q1MKX-1/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



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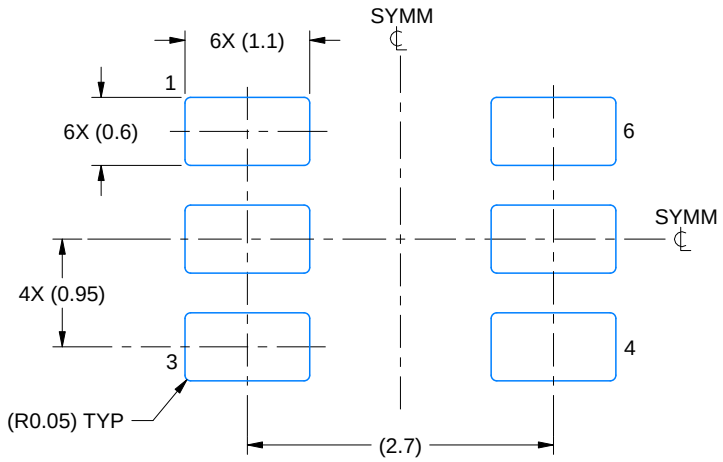
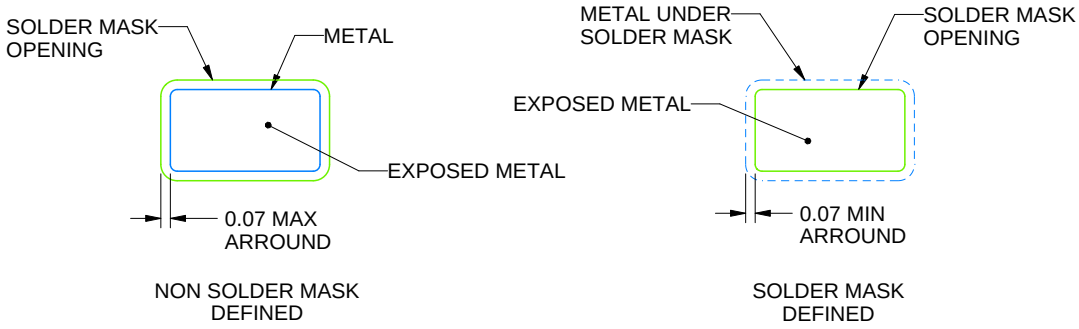
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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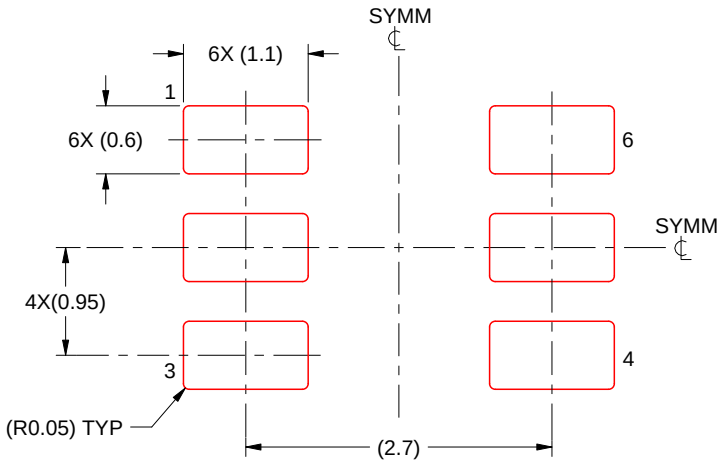
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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