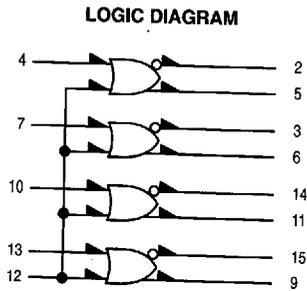


## Quad OR/NOR Gate

The MC10101 is a quad 2-input OR/NOR gate with one input from each gate common to pin 12.

$P_D = 25 \text{ mW typ/gate (No Load)}$   
 $t_{pd} = 2.0 \text{ ns typ}$   
 $t_r, t_f = 2.0 \text{ ns typ (20\%–80\%)}$



$V_{CC1} = \text{PIN 1}$   
 $V_{CC2} = \text{PIN 16}$   
 $V_{EE} = \text{PIN 8}$

# MC10101



**L SUFFIX**  
CERAMIC PACKAGE  
CASE 620-10

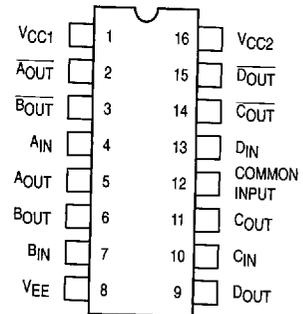


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08



**FN SUFFIX**  
PLCC  
CASE 775-02

### DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.  
For PLCC pin assignment, see the Pin Conversion Tables on page 6-11.

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits						Unit	
			-30°C		+25°C		+85°C			
			Min	Max	Min	Typ	Max	Min		Max
Power Supply Drain Current	I <sub>E</sub>	8		29		20	26		29	mAdc
Input Current	I <sub>inH</sub>	4 12		425 850			265 535		265 535	μAdc
	I <sub>inL</sub>	4 12	0.5 0.5		0.5 0.5			0.3 0.3		μAdc
Output Voltage Logic 1	VOH	5	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
		5	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
		2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
		2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	
Output Voltage Logic 0	VOL	5	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc
		5	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	
		2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	
		2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	
Threshold Voltage Logic 1	VOHA	5	-1.080		-0.980			-0.910		Vdc
		5	-1.080		-0.980			-0.910		
		2	-1.080		-0.980			-0.910		
		2	-1.080		-0.980			-0.910		
Threshold Voltage Logic 0	VOLA	5		-1.655			-1.630		-1.595	Vdc
		5		-1.655			-1.630		-1.595	
		2		-1.655			-1.630		-1.595	
		2		-1.655			-1.630		-1.595	
Switching Times (50Ω Load)									ns	
Propagation Delay	t <sub>4+2-</sub> t <sub>4-2+</sub> t <sub>4+5+</sub> t <sub>4-5-</sub>	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
		2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
		5	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
		5	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
Rise Time (20 to 80%)	t <sub>2+</sub> t <sub>5+</sub>	2	1.1	3.6	1.1	2.0	3.3	1.1	3.7	
		5	1.1	3.6	1.1	2.0	3.3	1.1	3.7	
Fall Time (20 to 80%)	t <sub>2-</sub> t <sub>5-</sub>	2	1.1	3.6	1.1	2.0	3.3	1.1	3.7	
		5	1.1	3.6	1.1	2.0	3.3	1.1	3.7	

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**ELECTRICAL CHARACTERISTICS** (continued)

② Test Temperature			TEST VOLTAGE VALUES (Volts)					(V <sub>CC</sub> ) Gnd	
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>		
-30°C			-0.890	-1.890	-1.205	-1.500	-5.2		
+25°C			-0.810	-1.850	-1.105	-1.475	-5.2		
+85°C			-0.700	-1.825	-1.035	-1.440	-5.2		
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>		
Power Supply Drain Current	I <sub>E</sub>	8					8	1, 16	
Input Current	I <sub>inH</sub>	4	4				8	1, 16	
		12	12				8	1, 16	
	I <sub>inL</sub>	4		4			8	1, 16	
		12		12			8	1, 16	
Output Voltage	Logic 1	V <sub>OH</sub>	5	12				8	1, 16
			5	4				8	1, 16
			2					8	1, 16
			2					8	1, 16
Output Voltage	Logic 0	V <sub>OL</sub>	5					8	1, 16
			5					8	1, 16
			2	12				8	1, 16
			2	4				8	1, 16
Threshold Voltage	Logic 1	V <sub>OHA</sub>	5		12			8	1, 16
			5		4			8	1, 16
			2			12		8	1, 16
			2			4		8	1, 16
Threshold Voltage	Logic 0	V <sub>OLA</sub>	5			12		8	1, 16
			5			4		8	1, 16
			2		12			8	1, 16
			2		4			8	1, 16
Switching Times	(50Ω Load)								
Propagation Delay	t <sub>4+2-</sub> t <sub>4-2+</sub> t <sub>4+5+</sub> t <sub>4-5-</sub>	2				Pulse In	Pulse Out	-3.2 V	+2.0 V
						4	2	8	1, 16
						4	2	8	1, 16
						4	5	8	1, 16
Rise Time	(20 to 80%)	t <sub>2+</sub> t <sub>5+</sub>	2	5		4	2	8	1, 16
Fall Time	(20 to 80%)	t <sub>2-</sub> t <sub>5-</sub>	2	5		4	2	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

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