TEXAS INSTRUMENTS
OPA191, OPA2191, OPA4191
SBOS701D – DECEMBER 2015 – REVISED AUGUST 2021

OPAx191 36-V, Low-Power, Precision, CMOS, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp

1 Features

- Low offset voltage: ±5 µV
- Low offset voltage drift: ±0.1 µV/°C
- Low noise: 15 nV/√Hz at 1 kHz
- High common-mode rejection: 140 dB
- Low bias current: ±5 pA
- Rail-to-rail input and output
- Wide bandwidth: 2.5-MHz GBW
- High slew rate: 5 V/µs
- Low quiescent current: 140 µA per amplifier
- Wide supply: ±2.25 V to ±18 V, 4.5 V to 36 V
- EMI/RFI filtered inputs
- Differential input voltage range to supply rail
- High capacitive load drive capability: 1 nF
- Industry standard packages:
  - Single in SOIC-8, SOT-5, and VSSOP-8
  - Dual in SOIC-8 and VSSOP-8
  - Quad in SOIC-14, TSSOP-14, and WQFN-16

2 Applications

- Analog input module
- Mixed module (AI, AO, DI, DO)
- Data acquisition (DAQ)
- Source measurement unit (SMU)
- Pressure transmitter
- Train control and management systems
- Lab and field instrumentation

3 Description

The OPAx191 family (OPA191, OPA2191, and OPA4191) is a new generation of 36-V, e-trim™ operational amplifiers.

These devices offer outstanding dc precision and ac performance, including rail-to-rail input/output, low offset voltage (±5 µV, typ), low offset drift (±0.2 µV/°C, typ), and 2-MHz bandwidth.

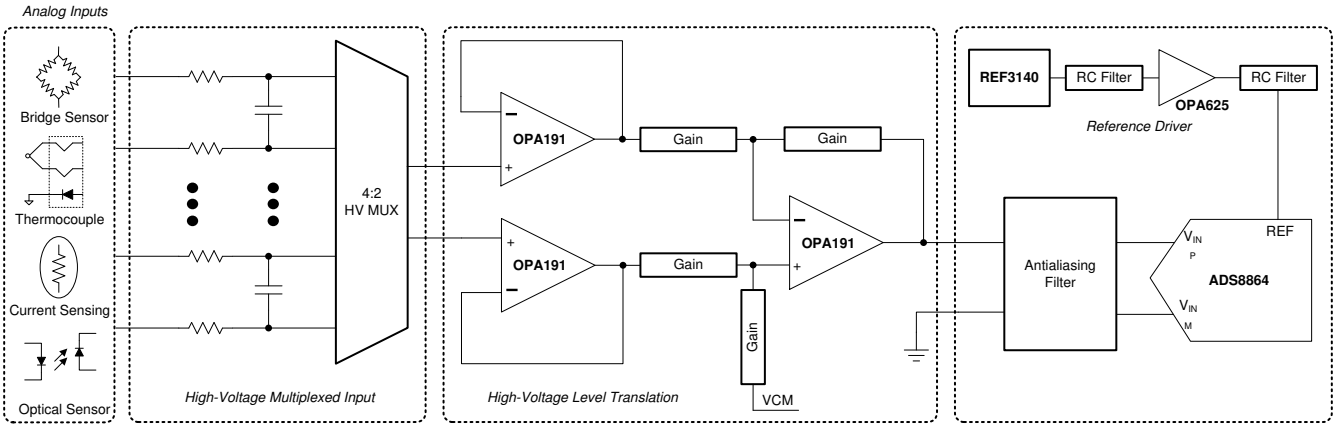
Unique features, such as differential input-voltage range to the supply rail, high output current (±65 mA), high capacitive load drive of up to 1 nF, and high slew rate (5 V/µs), make the OPAx191 a robust, high-performance operational amplifier for high-voltage industrial applications.

The OPAx191 family of op amps is available in standard packages and is specified from –40°C to +125°C.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
OPA191	SOIC (8)	4.90 mm × 3.90 mm
	SOT (5)	2.90 mm × 1.60 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA2191	SOIC (8)	4.90 mm × 3.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA4191	SOIC (14)	8.65 mm x 3.90 mm
	TSSOP (14)	5.00 mm x 4.40 mm
	WQFN (16)	4.00 mm x 4.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



OPA191 in a High-Voltage, Multiplexed, Data-Acquisition System

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2019) to Revision D (August 2021)	Page
• Changed OPA4191 PW (TSSOP-14) package from preview to production data (active)	1

Changes from Revision B (July 2019) to Revision C (October 2019)	Page
• Changed OPA4191 RUM package from preview to production data (active)	1

Changes from Revision A (April 2016) to Revision B (July 2019)	Page
• Added advanced information (preview) 16-pin RUM (WQFN) package and associated content to data sheet	1
• Changed Figure 32 condition from G = –1 to G = 1	11
• Changed Figure 33 condition from G = 1 to G = –1	11

Changes from Revision * (December 2015) to Revision A (April 2016)	Page
• Changed DBV and DGK packages from product preview to production data	1
• Changed Figure 23, 0.1-Hz to 10-Hz Noise	11
• Added text regarding capacitive load drive to the *Capacitive Load and Stability* section	26
• Added Figure 56	26

5 Pin Configuration and Functions

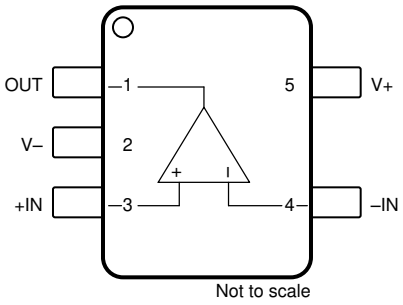

Figure 5-1. OPA191 DBV (5-Pin SOT) Package, Top View

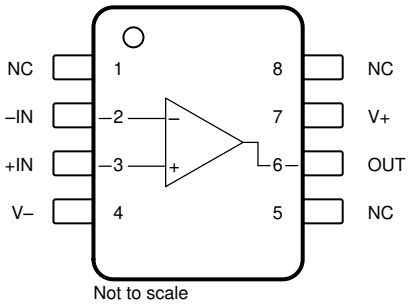

Figure 5-2. OPA191 D (8-Pin SOIC) and DGK (8-Pin VSSOP) Packages, Top View

Pin Functions: OPA191

PIN			I/O	DESCRIPTION
NAME	OPA191			
	D (SOIC), DGK (VSSOP)	DBV (SOT)		
+IN	3	3	I	Noninverting input
–IN	2	4	I	Inverting input
NC	1, 5, 8	—	—	No internal connection (can be left floating)
OUT	6	1	O	Output
V+	7	5	—	Positive (highest) power supply
V–	4	2	—	Negative (lowest) power supply

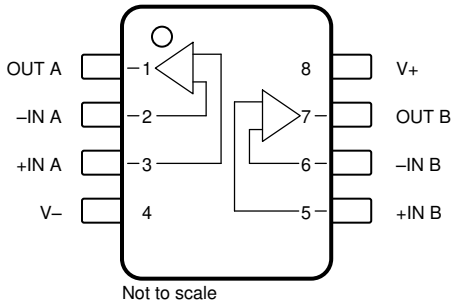

Figure 5-3. OPA2191 D (8-Pin SOIC) and DGK (8-Pin VSSOP) Packages, Top View

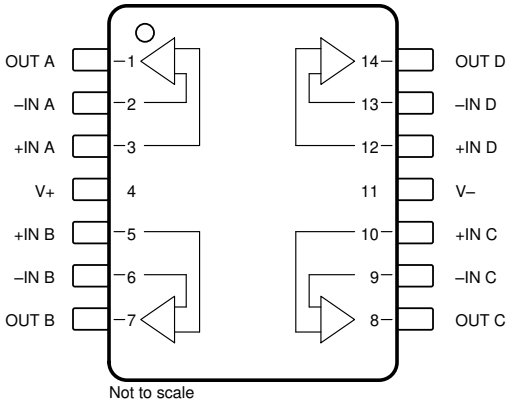

Figure 5-4. OPA4191 D (14-Pin SOIC) and PW (14-Pin TSSOP) Packages, Top View

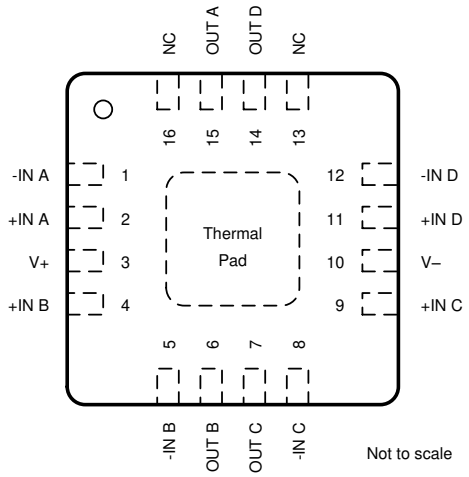

Figure 5-5. OPA4191 RUM (16-Pin WQFN With Exposed Thermal Pad) Package, Top View

Pin Functions: OPA2191 and OPA4191

PIN				I/O	DESCRIPTION
NAME	OPA2191	OPA4191			
	D (SOIC), DGK (VSSOP)	D (SOIC), PW (TSSOP)	RUM (QFN)		
+IN A	3	3	2	I	Noninverting input, channel A
+IN B	5	5	4	I	Noninverting input, channel B
+IN C	—	10	9	I	Noninverting input, channel C
+IN D	—	12	11	I	Noninverting input, channel D
–IN A	2	2	1	I	Inverting input, channel A
–IN B	6	6	5	I	Inverting input, channel B
–IN C	—	9	8	I	Inverting input,,channel C
–IN D	—	13	12	I	Inverting input, channel D
OUT A	1	1	15	O	Output, channel A
OUT B	7	7	6	O	Output, channel B
OUT C	—	8	7	O	Output, channel C
OUT D	—	14	14	O	Output, channel D
V+	8	4	3	—	Positive (highest) power supply
V–	4	11	10	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)				±20 (+40, single supply)	V
Signal input pins	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current			±10	mA
Output short circuit(2)			Continuous	Continuous	Continuous
Temperature	Operating		–40	150	°C
	Junction			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2), OPA4191IPW package only	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature	–40		125	°C

6.4 Thermal Information: OPA191

THERMAL METRIC[1]		OPA191			UNIT
		D (SOIC)	DGK (VSSOP)	DBV (SOT)	
		8 PINS		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.8	180.4	158.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	60.1	67.9	60.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.4	102.1	44.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.8	10.4	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.9	100.3	4.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: OPA2191

THERMAL METRIC[1]		OPA2191		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.9	158	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	53.9	48.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.9	78.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.3	77.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Thermal Information: OPA4191

THERMAL METRIC[1]		OPA4191			UNIT
		D (SOIC)	PW (TSSOP)	RUM (QFN)	
		14 PINS		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.4	108.1	33.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	46.3	26.3	25.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.0	54.4	11.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.3	1.4	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.7	53.3	11.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.7 Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V)

at T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±18 V			±5	±25	µV
			T_A = 0°C to 85°C		±8	±75	
			T_A = –40°C to +125°C		±10	±125	
		(V+) – 3.0 V < V_{CM} < (V+) – 1.5 V			See Typical Characteristics		
		V_S = ±18 V, V_{CM} = (V+) – 1.5 V			±10	±50	
			T_A = 0°C to 85°C		±25	±150	
			T_A = –40°C to +125°C		±50	±250	
		OPA4191 (RUM, PW), V_S = ±18 V VCM = (V+) – 1.5 V			±5	±50	
			T_A = 0°C to 85°C		±10	±475	
			TA = –40°C to +125°C		±20	±740	
dV_{OS}/dT	Input offset voltage drift	V_S = ±18 V, D and PW packages only	T_A = 0°C to 85°C		±0.1	±0.8	µV/°C
			T_A = –40°C to +125°C		±0.15	±1.2	
		V_S = ±18 V, RUM, DGK and DBV packages only	T_A = 0°C to 85°C		±0.1	±0.9	
			T_A = –40°C to +125°C		±0.15	±1.3	
		V_S = ±18 V, V_{CM} = (V+) – 1.5 V	T_A = –40°C to +125°C		±0.5		
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C			±0.3	±1.0	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to +125°C				±9	nA
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to +125°C				±2	nA
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 0.1 Hz to 10 Hz		1.4		μV_{PP}
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 0.1 Hz to 10 Hz		7		
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		18		$nV/\sqrt{Hz}$
			f = 1 kHz		15		
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		53		
			f = 1 kHz		24		
i_n	Input current noise density	f = 1 kHz			1.5		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 3 V		120	140		dB
		V_S = ±18 V, (V–) < V_{CM} < (V+) – 3 V	T_A = –40°C to +125°C	114	126		
		V_S = ±18 V, (V+) – 1.5 V < V_{CM} < (V+)		96	120		
			T_A = –40°C to +125°C	86	100		
		(V+) – 3 V < V_{CM} < (V+) – 1.5 V		See Typical Characteristics			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF

6.7 Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V) (continued)

at T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = ±18 V, (V–) + 0.6 V < V_O < (V+) – 0.6 V, R_L = 2 kΩ		124	134		dB
		V_S = ±18 V, (V–) + 0.8 V < V_O < (V+) – 0.8 V, R_L = 2 kΩ, RUM package		124	134		
		V_S = ±18 V, (V–) + 0.6 V < V_O < (V+) – 0.6 V, R_L = 2 kΩ	T_A = –40°C to +125°C	114	126		
		V_S = ±18 V, (V–) + 0.8 V < V_O < (V+) – 0.8 V, R_L = 2 kΩ, RUM package	T_A = –40°C to +125°C	114	126		
		V_S = ±18 V, (V–) + 0.3 V < V_O < (V+) – 0.3 V, R_L = 10 kΩ		126	140		
		V_S = ±18 V, (V–) + 0.3 V < V_O < (V+) – 0.3 V, R_L = 10 kΩ	T_A = –40°C to +125°C	120	134		
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				2.5		MHz
SR	Slew rate	V_S = ±18 V, G = 1, 10-V step	Falling		7.5		V/µs
			Rising		5.5		
t_s	Settling time	To 0.01%, C_L = 20 pF	V_S = ±18 V, G = 1, 2-V step		0.7		µs
			V_S = ±18 V, G = 1, 5-V step		1		
		To 0.001%, C_L = 20 pF	V_S = ±18 V, G = 1, 2-V step		1.8		
			V_S = ±18 V, G = 1, 5-V step		3.7		
t_{OR}	Overload recovery time	V_{IN} × G = V_S	From overload to negative rail		0.4		µs
			From overload to positive rail		1		
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.0012%		
	Crosstalk	OPA2191 and OPA4191, at dc			150		dB
		OPA2191 and OPA4191, f = 100 kHz			130		dB
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_L = 10 kΩ		50	110	
			R_L = 2 kΩ		200	500	
		Negative rail	No load		5	15	
			R_L = 10 kΩ		50	110	
			R_L = 2 kΩ		200	500	
I_{SC}	Short-circuit current	V_S = ±18 V			±65		mA
C_L	Capacitive load drive				See Typical Characteristics		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A, See Typical Characteristics			700		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			140	200	µA
			T_A = –40°C to +125°C			250	
TEMPERATURE							
	Thermal protection				180		°C
	Thermal hysteresis				30		°C

6.8 Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = 4.5 V to 8 V)

at T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±2.25 V, V_{CM} = (V+) – 3 V			±5	±25	μV
			T_A = 0°C to 85°C		±8	±75	
			T_A = –40°C to +125°C		±10	±125	
		(V+) – 3.0 V < V_{CM} < (V+) – 1.5 V			See Typical Characteristics		
		V_S = ±3 V, V_{CM} = (V+) – 1.5 V			±10	±50	
			T_A = 0°C to 85°C		±25	±150	
			T_A = –40°C to +125°C		±50	±250	
		OPA4191 (RUM, PW), V_S = ±3 V, V_{CM} = (V+) – 1.5 V			±10	±50	
			T_A = –40°C to +85°C		±90	±475	
			T_A = –40°C to +125°C		±150	±740	
dV_{OS}/dT	Input offset voltage drift	V_S = ±2.25 V, V_{CM} = (V+) – 3 V, D and PW packages only	T_A = 0°C to 85°C		±0.1	±0.8	μV/°C
			T_A = –40°C to +125°C		±0.15	±1.2	μV/°C
		V_S = ±2.25 V, V_{CM} = (V+) – 3 V, RUM, DGK and DBV packages only	T_A = 0°C to 85°C		±0.1	±0.9	μV/°C
			T_A = –40°C to +125°C		±0.15	±1.3	
		V_S = ±2.25 V, V_{CM} = (V+) – 1.5 V	T_A = –40°C to +125°C		±0.5		
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C, V_{CM} = V_S / 2 – 0.75 V			±1		μV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to +125°C				±9	nA
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to +125°C				±2	nA
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 0.1 Hz to 10 Hz		1.4		$μV_{PP}$
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 0.1 Hz to 10 Hz		7		
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		18		$nV/\sqrt{Hz}$
			f = 1 kHz		15		
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		53		
			f = 1 kHz		24		
i_n	Input current noise density		f = 1 kHz		1.5		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = ±2.25 V, (V–) – 0.1 V < V_{CM} < (V+) – 3 V		96	110		dB
		V_S = ±2.25 V, (V–) < V_{CM} < (V+) – 3 V	T_A = –40°C to +125°C	90	104		
		V_S = ±2.25 V, (V+) – 1.5 V < V_{CM} < (V+)		96	120		
			T_A = –40°C to +125°C	84	100		
		(V+) – 3 V < V_{CM} < (V+) – 1.5 V		See Typical Characteristics			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF

6.8 Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = 4.5 V to 8 V) (continued)

at T_A = +25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = ±2.25 V, (V–) + 0.6 V < V_O < (V+) – 0.6 V, R_L = 2 kΩ		110	120		dB
			T_A = –40°C to +125°C	100	114		
		V_S = ±2.25 V, (V–) + 0.3 V < V_O < (V+) – 0.3 V, R_L = 10 kΩ		110	126		
			T_A = –40°C to +125°C	106	120		
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				2.2		MHz
SR	Slew rate	V_S = ±2.25 V, G = 1, 1-V step	Falling		6.5		V/µs
			Rising		5.5		
t_{OR}	Overload recovery time	V_{IN} × G = V_S	From overload to negative rail		0.4		µs
			From overload to positive rail		1		
	Crosstalk	OPA2191 and OPA4191, at dc			150		dB
		OPA2191 and OPA4191, f = 100 kHz			130		dB
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_L = 10 kΩ		15	110	
			R_L = 2 kΩ		60	500	
		Negative rail	No load		5	15	
			R_L = 10 kΩ		15	110	
			R_L = 2 kΩ		60	500	
I_{SC}	Short-circuit current	V_S = ±2.25 V			±30		mA
C_L	Capacitive load drive				See Typical Characteristics		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A, see Typical Characteristics			700		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			140	200	µA
			T_A = –40°C to +125°C			250	
TEMPERATURE							
	Thermal protection				180		°C
	Thermal hysteresis				30		°C

6.9 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

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Small Signal Overshoot vs Capacitive Load (100-mV output step)	Figure 6-32, Figure 6-33
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6.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

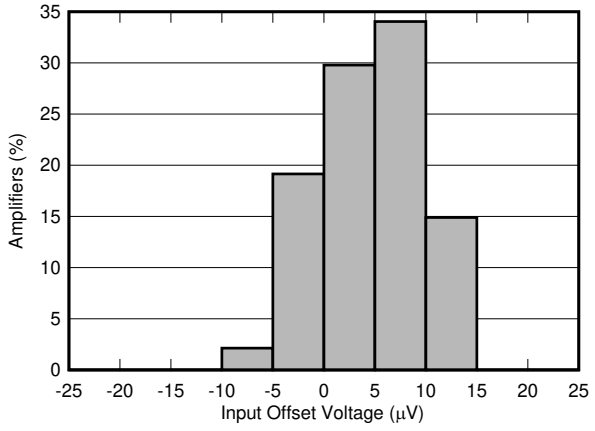


Figure 6-1. Offset Voltage Production Distribution

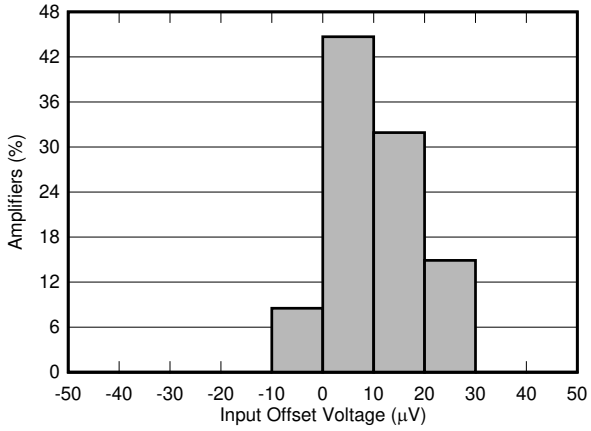


Figure 6-2. Offset Voltage Production Distribution

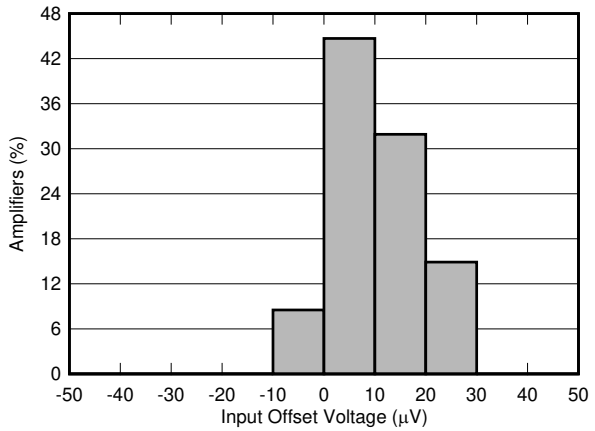


Figure 6-3. Offset Voltage Production Distribution

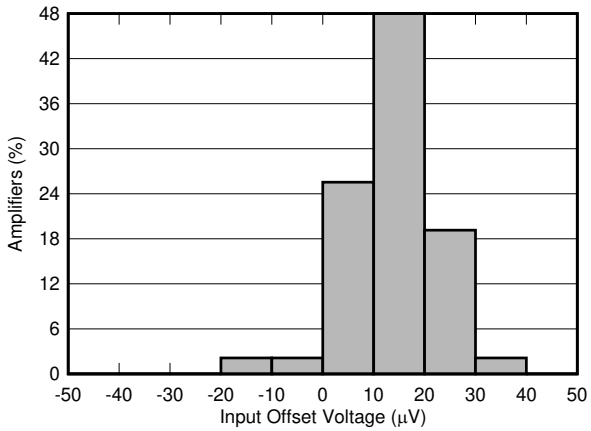


Figure 6-4. Offset Voltage Production Distribution

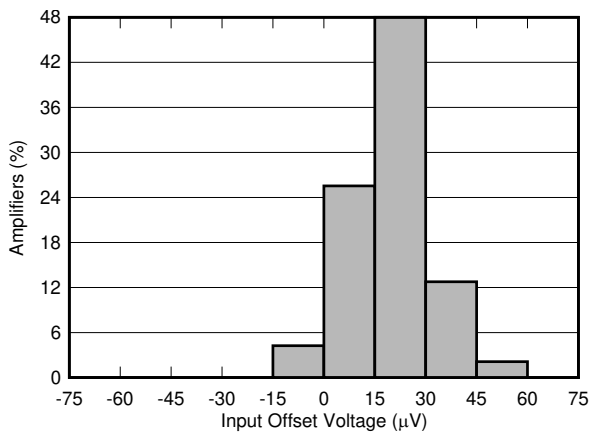


Figure 6-5. Offset Voltage Production Distribution

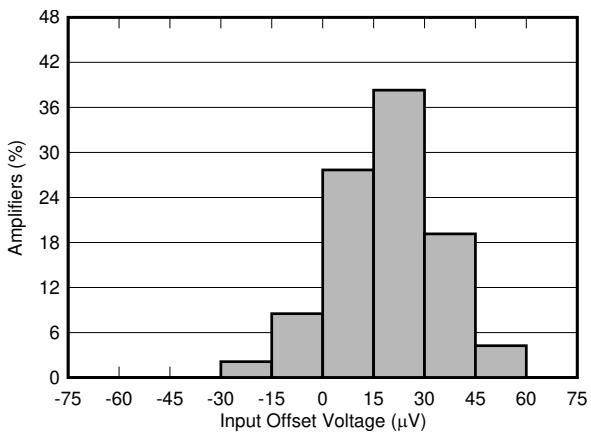
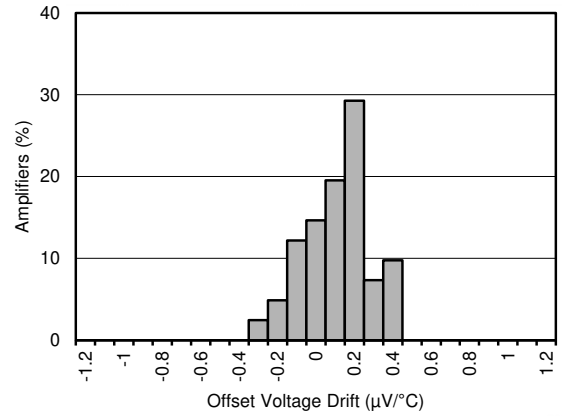


Figure 6-6. Offset Voltage Production Distribution

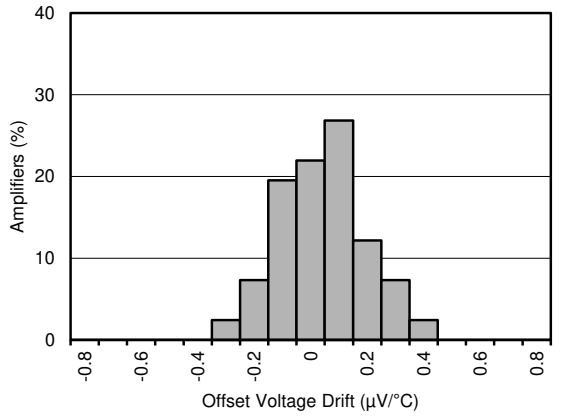
6.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



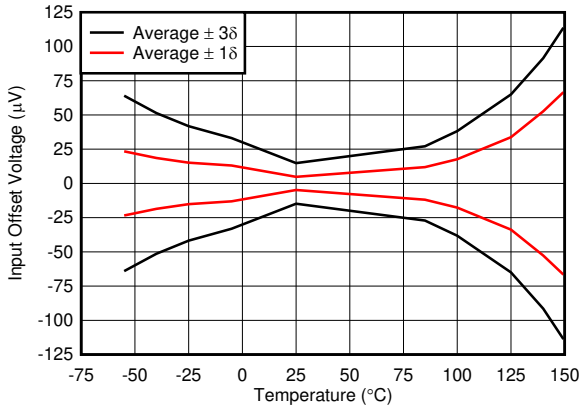
T_A = –40°C to +125°C, SOIC package

Figure 6-7. Offset Voltage Drift Distribution



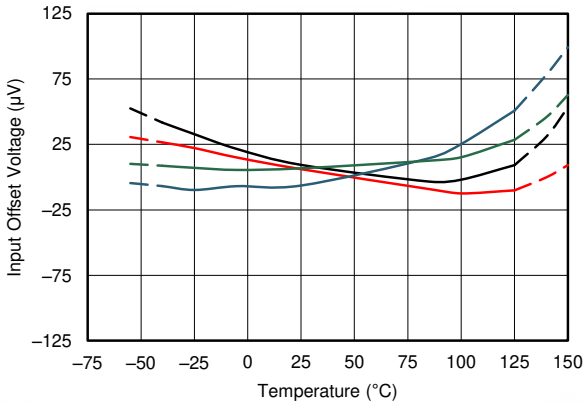
T_A = 0°C to 85°C, SOIC package

Figure 6-8. Offset Voltage Drift Distribution



Statistical distribution

Figure 6-9. Offset Voltage vs Temperature



4 typical units

Figure 6-10. Offset Voltage vs Temperature

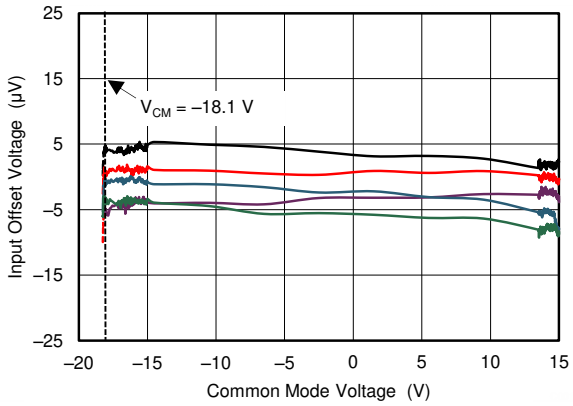


Figure 6-11. Offset Voltage vs Common-Mode Voltage

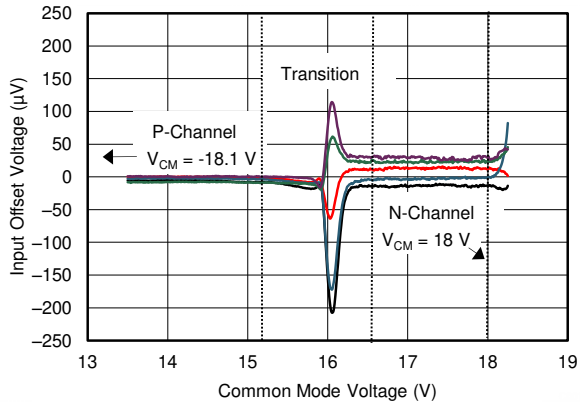


Figure 6-12. Offset Voltage vs Common-Mode Voltage in Transition Region

6.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

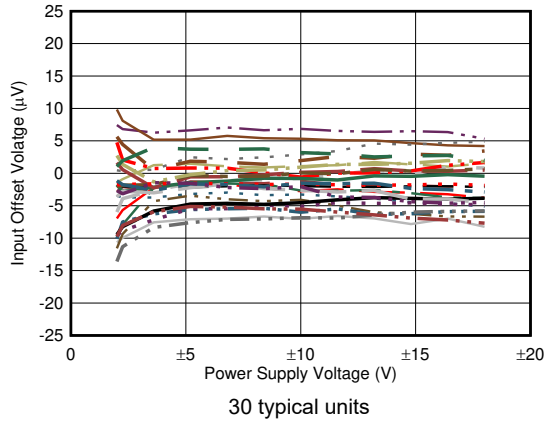


Figure 6-13. Offset Voltage vs Power Supply

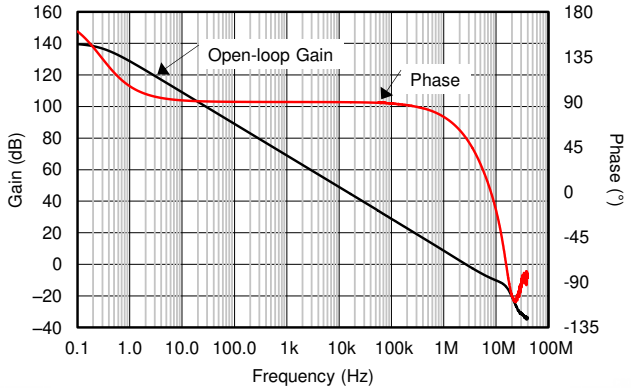


Figure 6-14. Open-Loop Gain and Phase vs Frequency

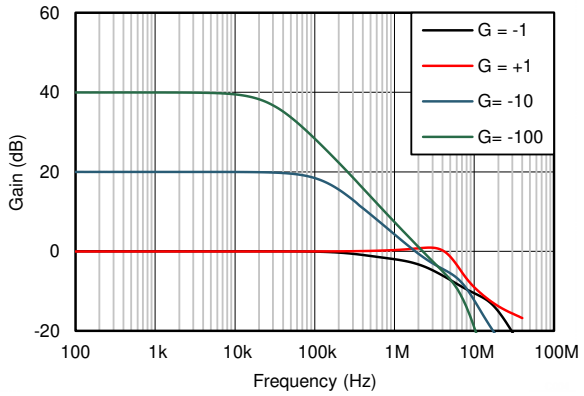


Figure 6-15. Closed-Loop Gain vs Frequency

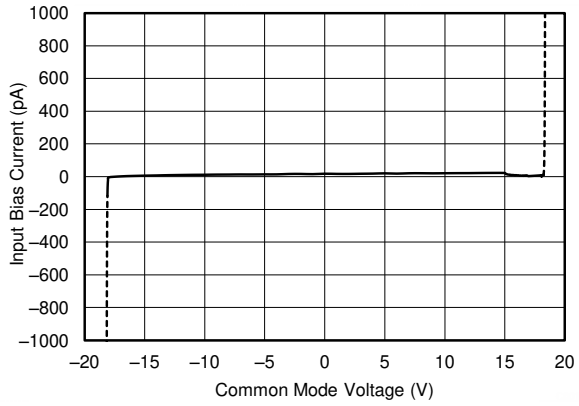


Figure 6-16. Input Bias Current vs Common-Mode Voltage

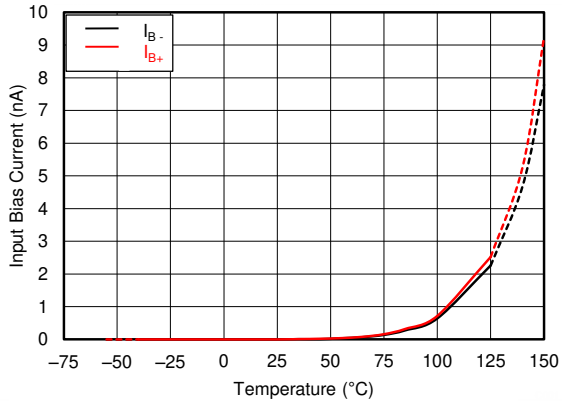


Figure 6-17. Input Bias Current vs Temperature

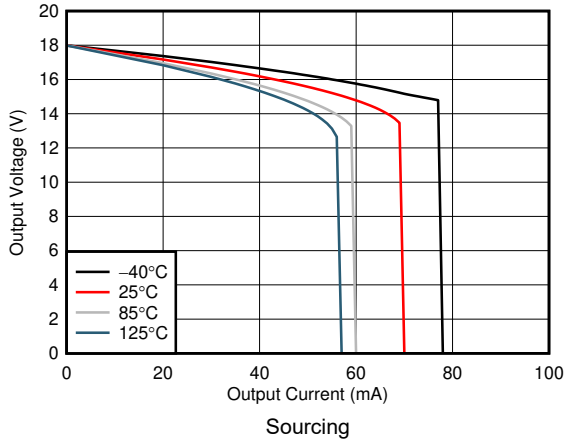


Figure 6-18. Output Voltage Swing vs Output Current

6.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

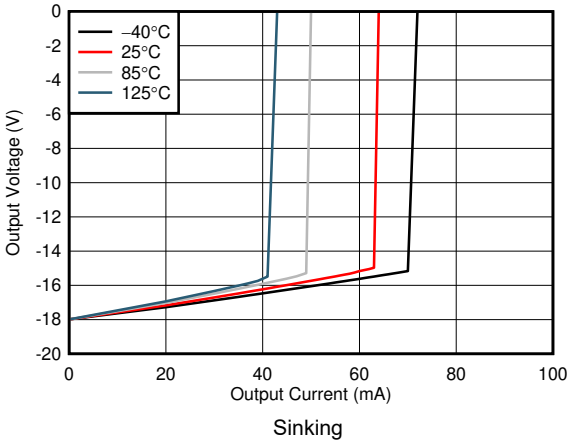


Figure 6-19. Output Voltage Swing vs Output Current

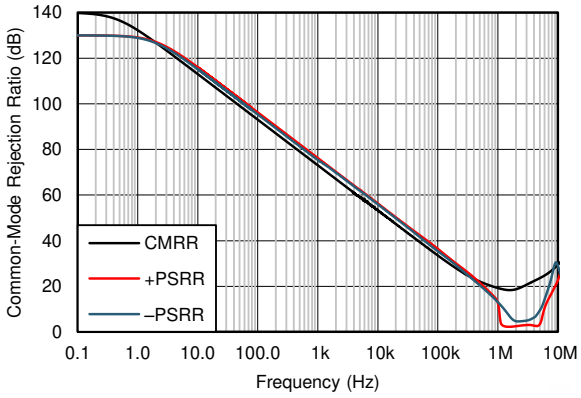


Figure 6-20. CMRR and PSRR vs Frequency

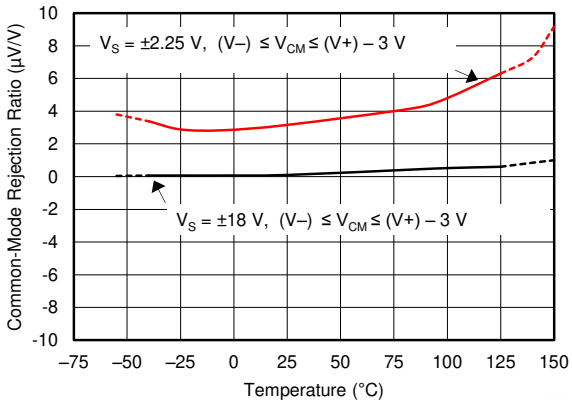


Figure 6-21. CMRR vs Temperature

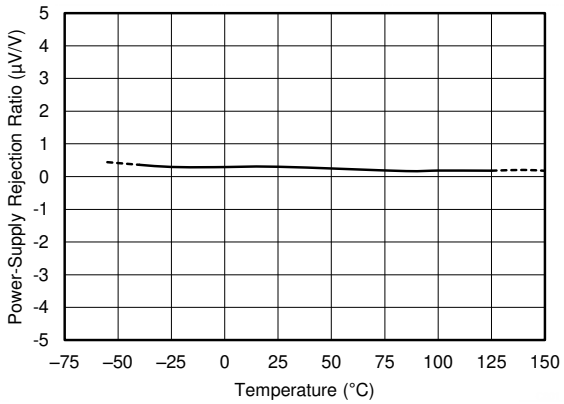


Figure 6-22. PSRR vs Temperature

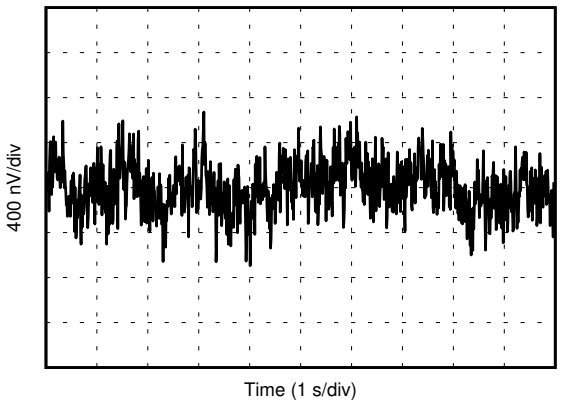


Figure 6-23. 0.1-Hz to 10-Hz Noise

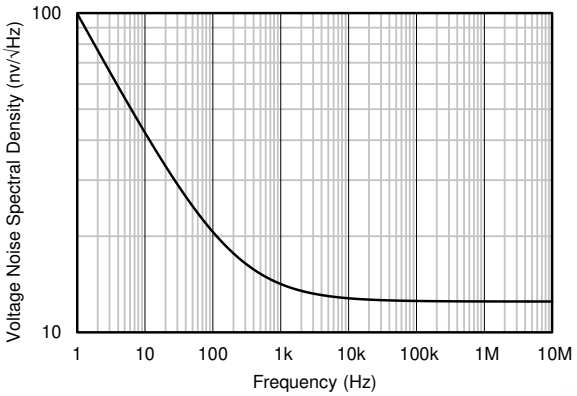


Figure 6-24. Input Voltage Noise Spectral Density vs Frequency

6.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

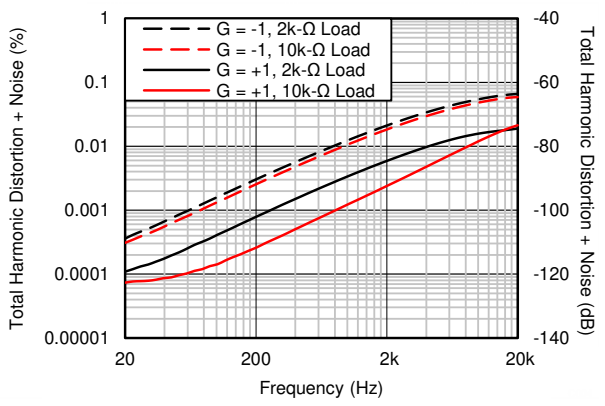


Figure 6-25. THD+N vs Frequency

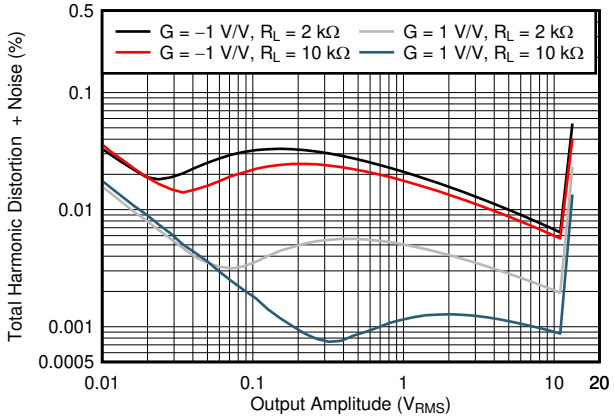


Figure 6-26. THD+N vs Output Amplitude

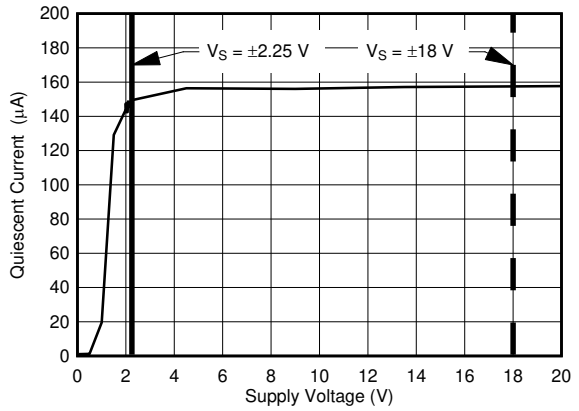


Figure 6-27. Quiescent Current vs Supply Voltage

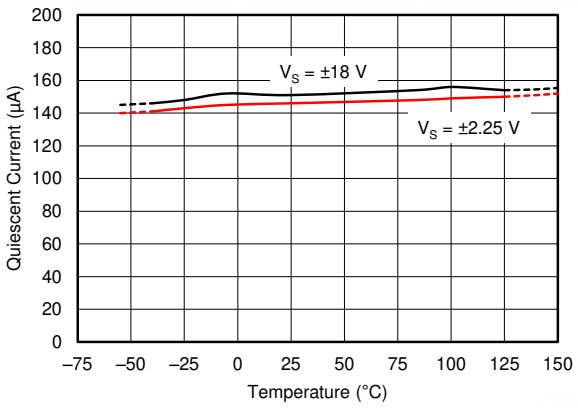
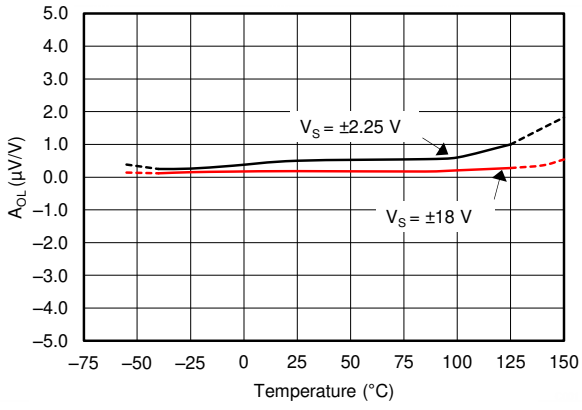
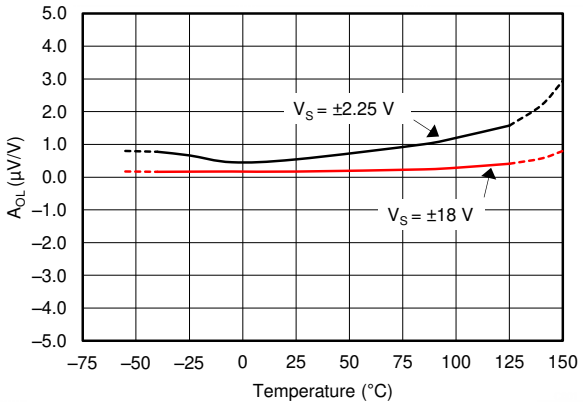


Figure 6-28. Quiescent Current vs Temperature



R_L = 10 kΩ

Figure 6-29. Open-Loop Gain vs Temperature



R_L = 2 kΩ

Figure 6-30. Open-Loop Gain vs Temperature

6.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

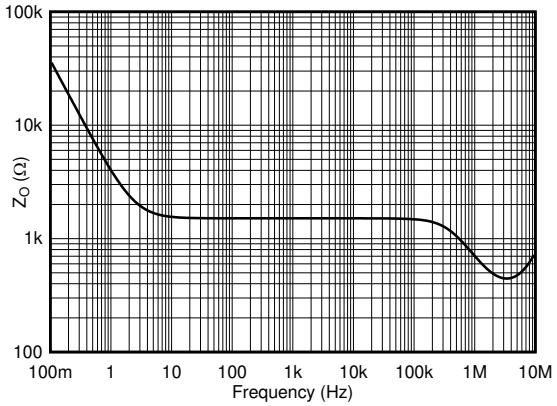
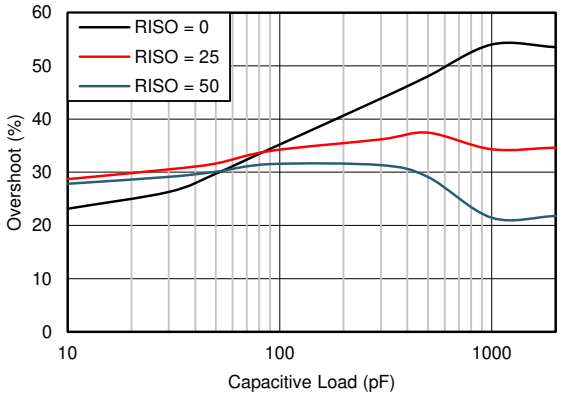
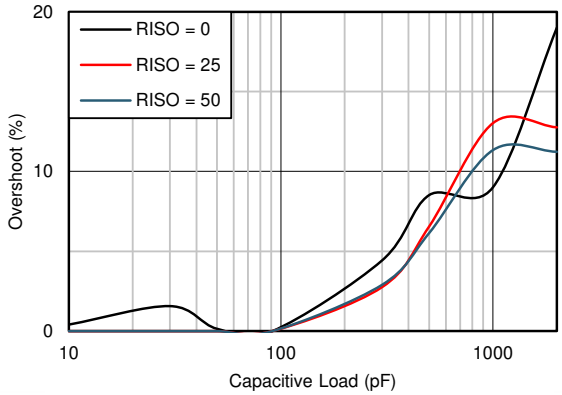


Figure 6-31. Open-Loop Output Impedance vs Frequency



G = 1, 100-mV output step

Figure 6-32. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)



G = –1, 100-mV output step

Figure 6-33. Small-Signal Overshoot vs Capacitive Load

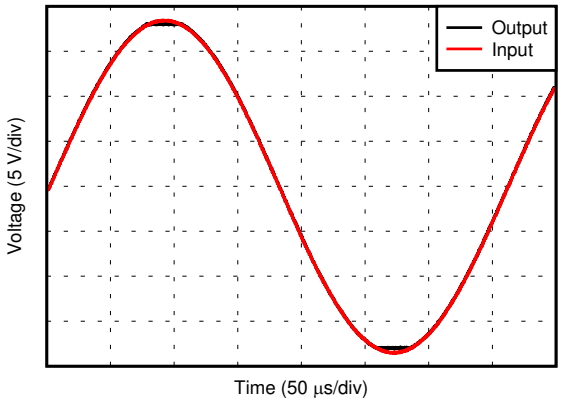
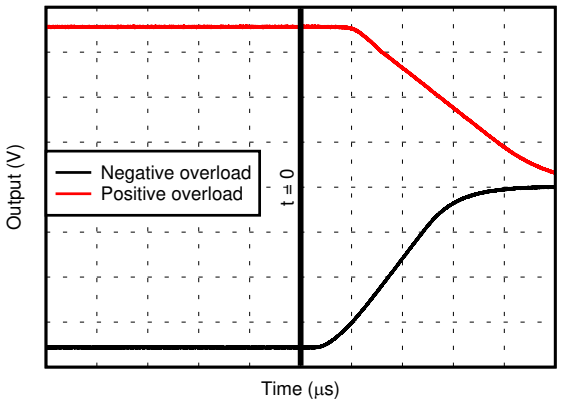
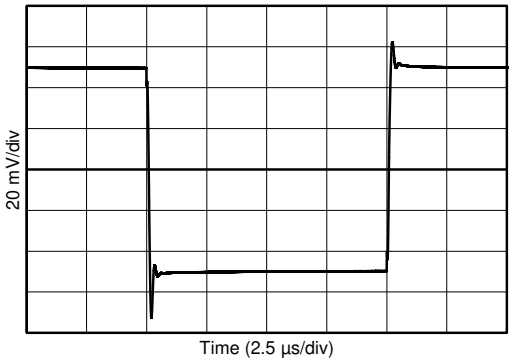


Figure 6-34. No Phase Reversal



V_S = ±18 V, G = –10 V/V

Figure 6-35. Overload Recovery

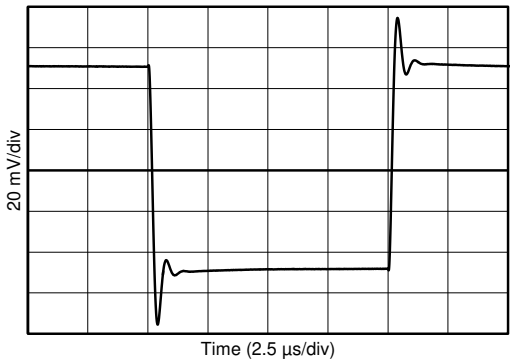


G = 1, C_L = 10 pF

Figure 6-36. Small-Signal Step Response

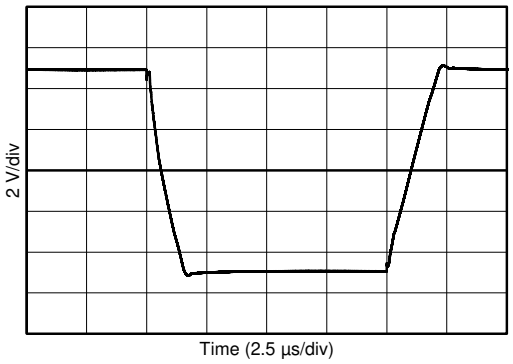
6.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



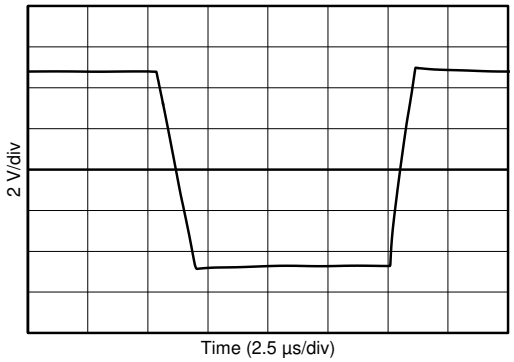
G = –1, R_L = 1 kΩ, C_L = 10 pF

Figure 6-37. Small-Signal Step Response



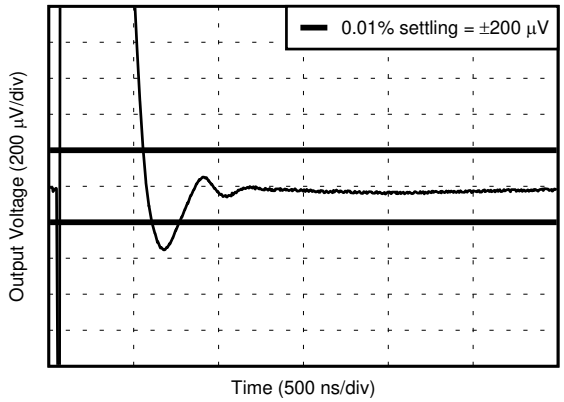
G = 1, C_L = 10 pF

Figure 6-38. Large-Signal Step Response



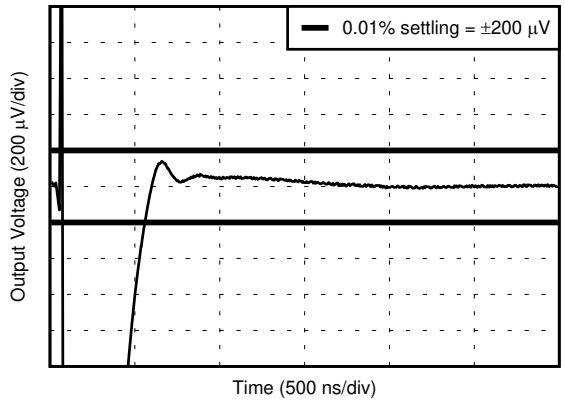
G = –1, R_L = 1 kΩ, C_L = 10 pF

Figure 6-39. Large-Signal Step Response



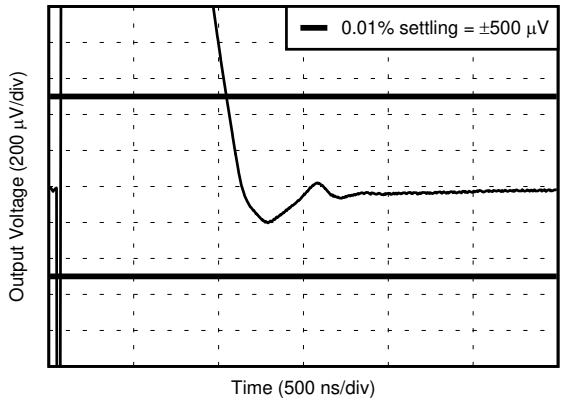
Gain = 1, 2-V step, rising, step applied at t = 0 µs

Figure 6-40. 0.01% Settling Time



Gain = 1, 2-V step, falling, step applied at t = 0 µs

Figure 6-41. 0.01% Settling Time

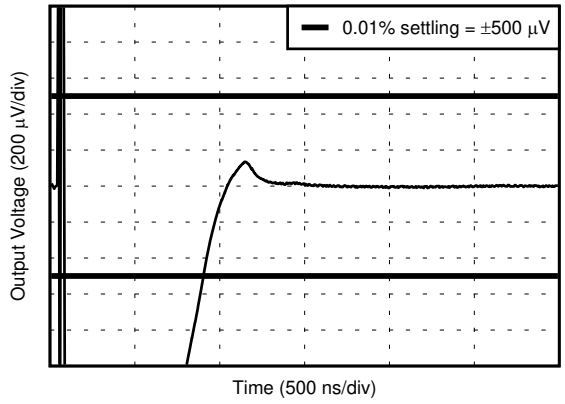


Gain = 1, 5-V step, rising, step applied at t = 0 µs

Figure 6-42. 0.01% Settling Time

6.9 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



Gain = 1, 5-V step, falling, step applied at t = 0 µs

Figure 6-43. 0.01% Settling Time

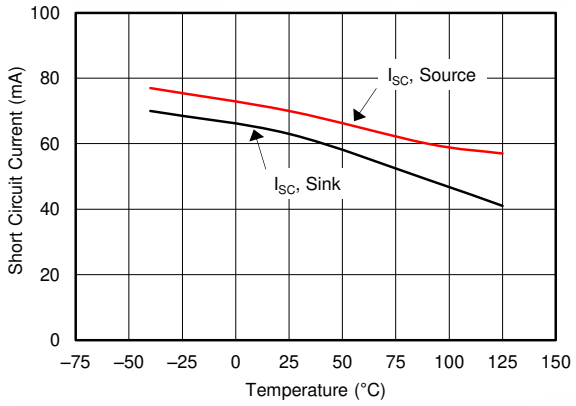


Figure 6-44. Short-Circuit Current vs Temperature

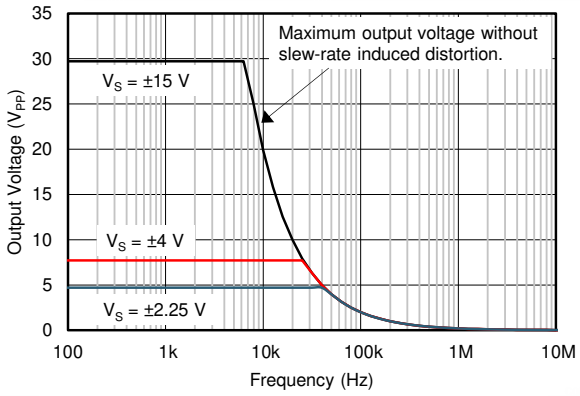


Figure 6-45. Maximum Output Voltage vs Frequency

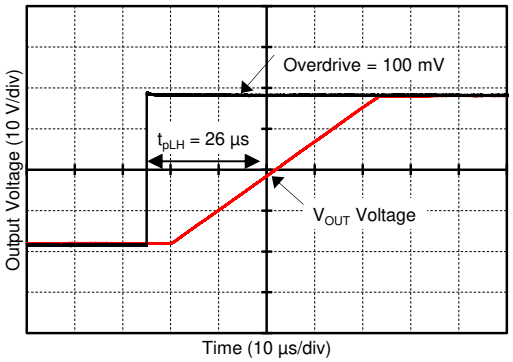


Figure 6-46. Propagation Delay Rising Edge

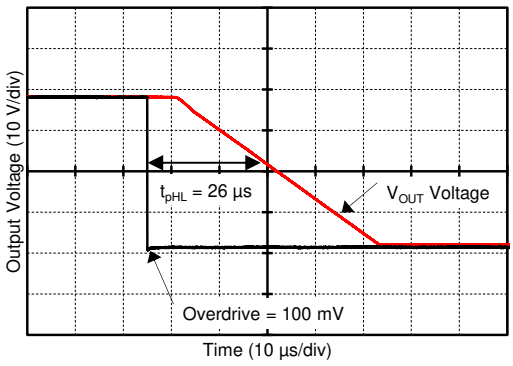


Figure 6-47. Propagation Delay Falling Edge

7 Parameter Measurement Information

7.1 Input Offset Voltage Drift

The OPAx191 family of operational amplifiers is manufactured using TI's *e-trim* operation amplifier technology. This e-trim operational amplifier technology is a TI proprietary method of trimming internal device parameters during either wafer probing or final testing. Each amplifier input offset voltage and input offset voltage drift is trimmed in production, thereby minimizing errors associated with input offset voltage and input offset voltage drift. When trimming input offset voltage drift, the systematic or linear drift error on each device is trimmed to zero. Figure 7-1 illustrates this concept.

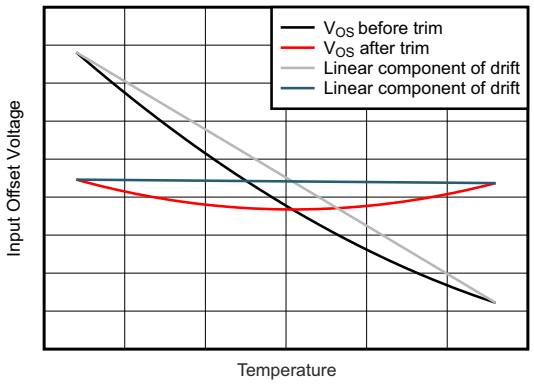


Figure 7-1. Input Offset Before and After Drift Trim

A common method of specifying input offset voltage drift is the *box method*. The box method estimates a maximum input offset drift by bounding an offset voltage versus temperature curve with a box and using the corners of this bounding box to determine the drift. The slope of the line connecting the diagonal corners of the box corresponds to the input offset voltage drift. Figure 7-2 illustrates the box method concept. The box method works particularly well when the input offset drift is dominated by the linear component of drift, but because the OPA191 family uses TI's e-trim operational amplifier technology to remove the linear component input offset voltage drift, the box method is not a particularly useful method of accurately performing an error analysis. Shown in Figure 7-2 are 30 typical units of OPAx191 with the box method superimposed for illustrative purposes. The boundaries of the box are determined by the specified temperature range along the x-axis and the maximum specified input offset voltage across that same temperature range along the y-axis. Using the box method predicts an input offset voltage drift of 0.9 µV/°C. As shown in Figure 7-2, the slopes of the actual input offset voltage versus temperature are much less than that predicted by the box method. The box method predicts a pessimistic value for the maximum input offset voltage drift and is not recommended when performing an error analysis.

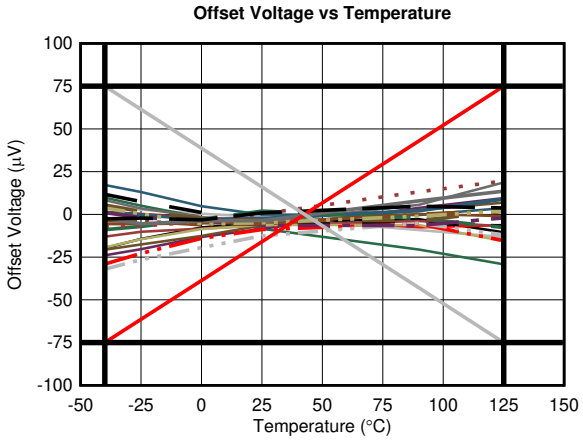


Figure 7-2. The Box Method

Instead of the box method, a convenient way to illustrate input offset drift is to compute the slopes of the input offset voltage versus temperature curve. This is the same as computing the input offset drift at each point along the input offset voltage versus temperature curve. The results for the OPAx191 family are illustrated in Figure 7-3.

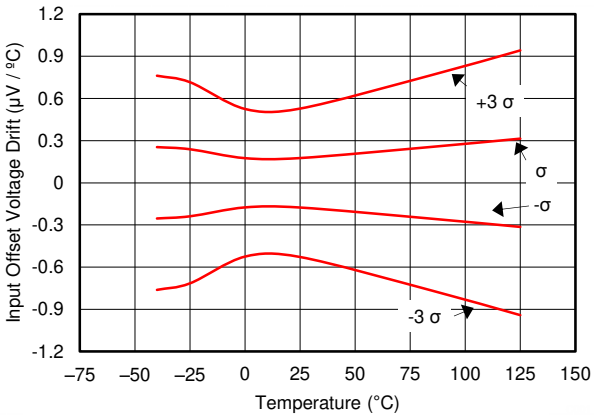


Figure 7-3. Input Offset Voltage Drift vs Temperature (SOIC Package)

As illustrated in Figure 7-3, the input offset drift is typically less than ±0.3 µV/°C over the range from –40°C to +125°C. When performing an error analysis over the full specified temperature range, use the typical and maximum values for input offset voltage drift as described in the *Electrical Characteristics* tables. If a reduced temperature range is applicable, use the information illustrated in Figure 7-3 when performing an error analysis. To determine the change in input offset voltage, use Equation 1:

$$\Delta V_{OS} = \Delta T \times dV_{OS}/dT \quad (1)$$

where

- ΔV_{OS} = Change in input offset voltage
- ΔT = Change in temperature
- dV_{OS}/dT = Input offset voltage drift

For example, determine the amount of OPA191ID input offset voltage change over the temperature range of 25°C to 75°C for 1 σ (68%) of the units. As shown in Figure 7-3, the input offset drift is typically 0.25 µV/°C. This input offset drift results in a typical input offset voltage change of (75°C – 25°C) × 0.25 µV/°C = 12.5 µV.

For 3 σ (99.7%) of the units, Figure 7-3 shows a typical input offset drift of approximately 0.75 µV/°C. This input offset drift results in a typical input offset voltage change of (75°C – 25°C) × 0.75 µV/°C = 37.5 µV.

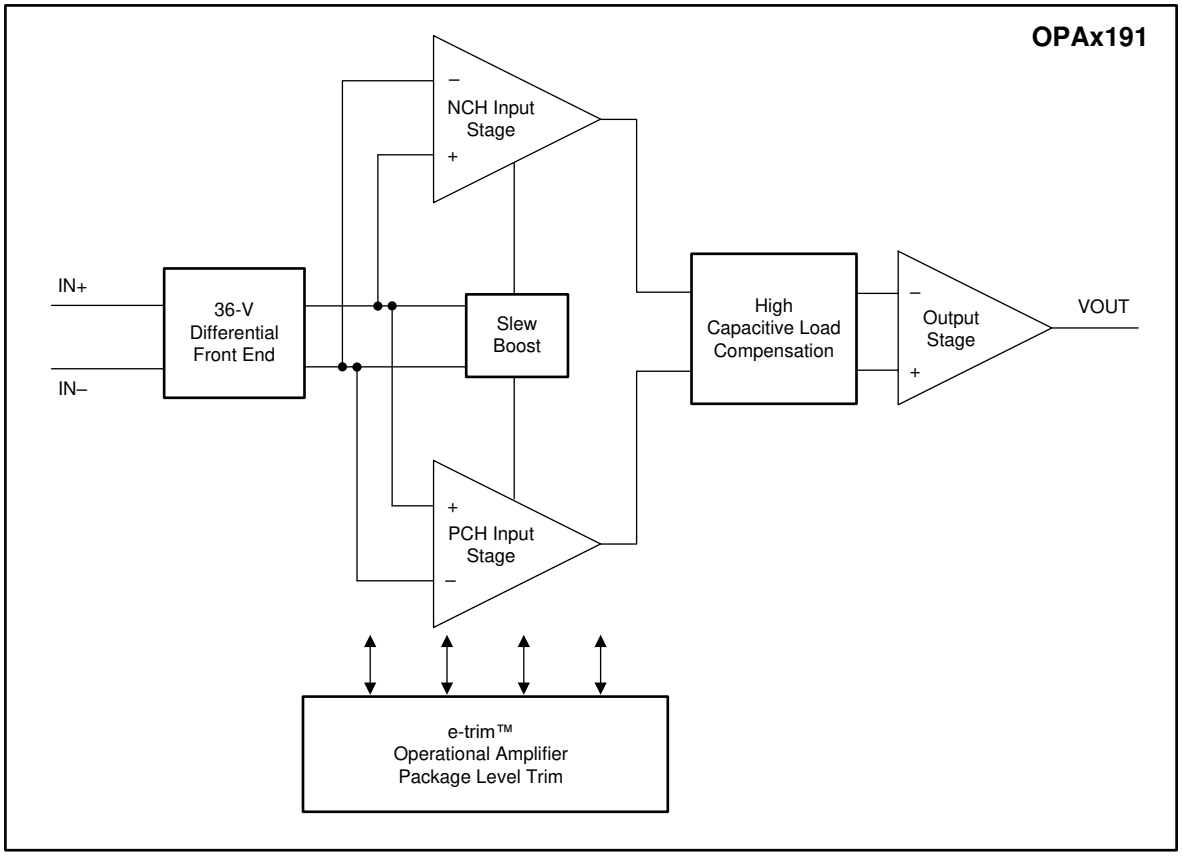
8 Detailed Description

8.1 Overview

The OPAx191 family of e-trim operational amplifiers use a method of package-level trim for offset and offset temperature drift implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent input transistor mismatch, as well as errors induced during package molding. The trim communication occurs on the output pin of the standard pinout, and after the trim points are set, further communication to the trim structure is permanently disabled. *Section 8.2* shows the simplified diagram of the OPAx191.

Unlike previous e-trim operational amplifiers, the OPAx191 uses a patented two-temperature trim architecture to achieve a very low offset voltage and low voltage offset drift over the full specified temperature range. This level of precision performance at wide supply voltages makes these amplifiers useful for high-impedance industrial sensors, filters, and high-voltage data acquisition.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Protection Circuitry

The OPAx191 uses a unique input architecture to eliminate the need for input protection diodes but still provides robust input protection under transient conditions. Conventional input diode protection schemes shown in Figure 8-1 can be activated by fast transient step responses and can introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 8-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes that cause an increase in input current, resulting in extended settling time.

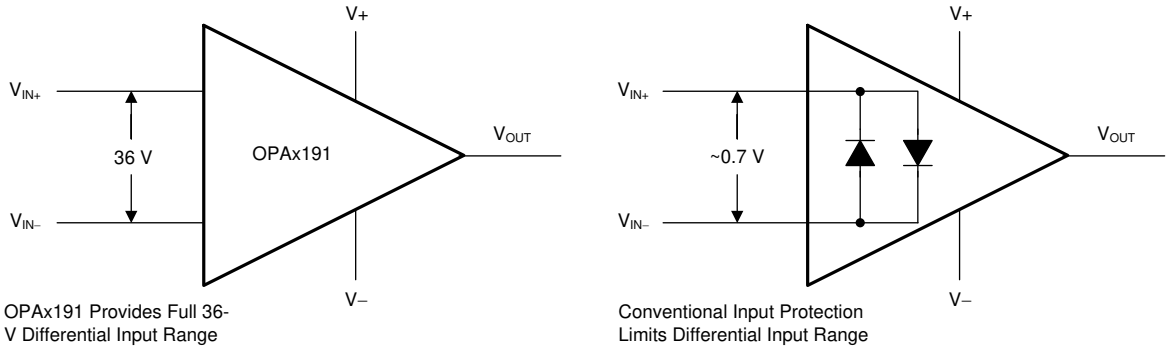


Figure 8-1. OPA191 Input Protection Does Not Limit Differential Input Capability

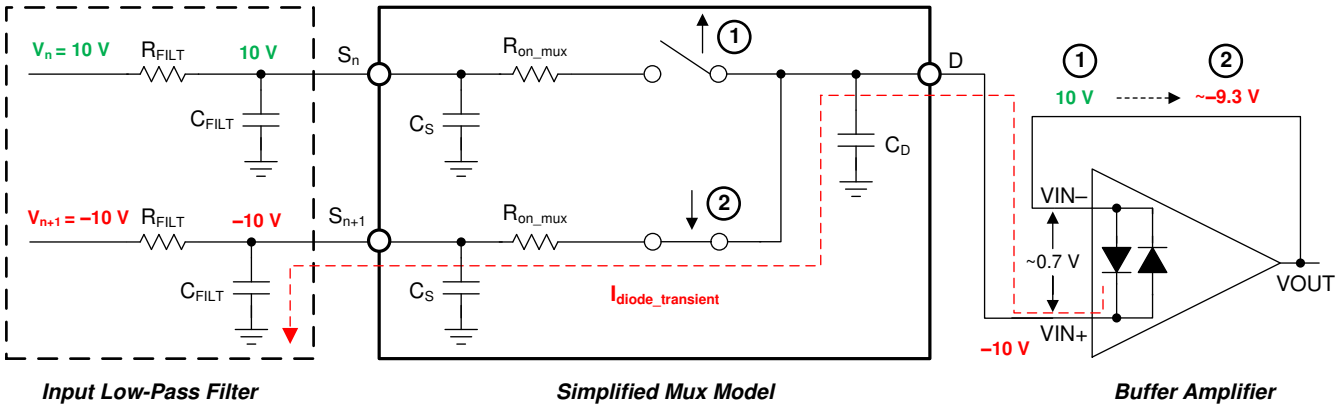
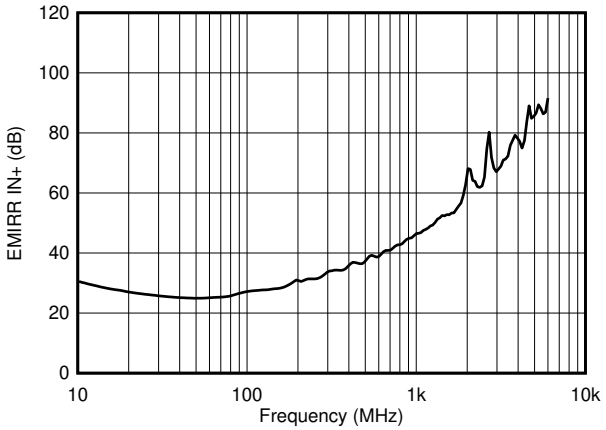


Figure 8-2. Back-to-Back Diodes Create Settling Issues

The OPAx191 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPAx191 tolerates a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 36 V, making the device an excellent choice for use as a comparator or in applications with fast-ramping input signals such as multiplexed data-acquisition systems (see Figure 9-4).

8.3.2 EMI Rejection

The OPAx191 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx191 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 8-3 shows the results of this testing on the OPAx191. Table 8-1 shows the EMIRR IN+ values for the OPAx191 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 8-1 may be centered on or operated near the particular frequency shown. Detailed information can also be found in the *EMI Rejection Ratio of Operational Amplifiers* application report , available for download from www.ti.com.



P_{RF} = –10 dBm, V_S = ±15 V, V_{CM} = 0 V

Figure 8-3. EMIRR Testing

Table 8-1. OPA191 EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	36 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	45 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	57 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	62 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	76 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	86 dB

8.3.3 Phase Reversal Protection

The OPAx191 family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx191 is a rail-to-rail input op amp, and therefore the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in Figure 8-4.

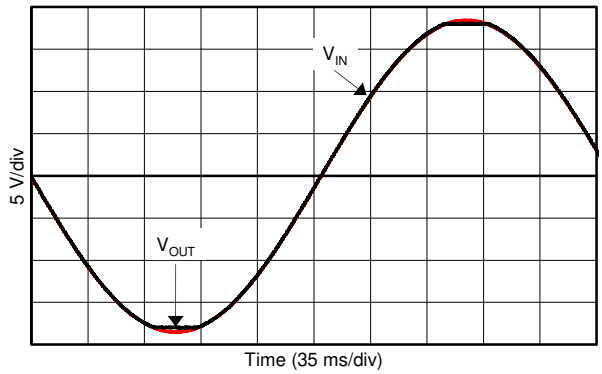


Figure 8-4. No Phase Reversal

8.3.4 Thermal Protection

The internal power dissipation of any amplifier causes the internal (junction) temperature to rise. This phenomenon is called *self heating*. The OPAx191 has a thermal protection feature that prevents damage from self heating.

This thermal protection works by monitoring the temperature of the output stage and turning off the op amp output drive for temperatures above approximately 180°C. Thermal protection forces the output to a high-impedance state. The OPAx191 is also designed with approximately 30°C of thermal hysteresis. Thermal hysteresis prevents the output stage from cycling in and out of the high-impedance state. The OPAx191 returns to normal operation when the output stage temperature falls below approximately 150°C.

The absolute maximum junction temperature of the OPAx191 is 150°C. Exceeding the limits shown in *Section 6.1* may cause damage to the device. Thermal protection triggers at 180°C because of unit-to-unit variance, but does not interfere with device operation up to the absolute maximum ratings. This thermal protection is not designed to prevent this device from exceeding absolute maximum ratings, but rather from excessive thermal overload.

8.3.5 Capacitive Load and Stability

The OPAx191 features a patented output stage capable of driving large capacitive loads, and in a unity-gain configuration, directly drives up to 1 nF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 8-5. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

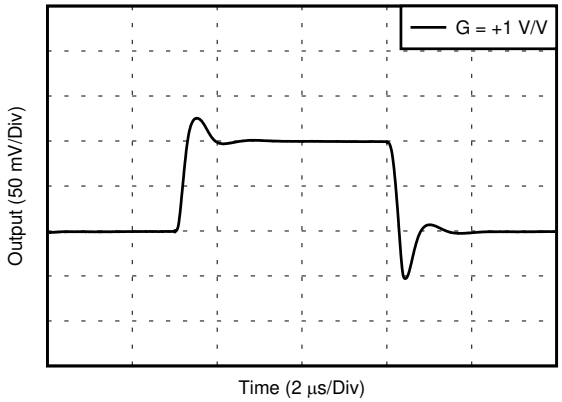


Figure 8-5. Transient Response with a Purely Capacitive Load of 1 nF

Like many low-power amplifiers, some ringing can occur even with capacitive loads less than 100 pF. In unity-gain configurations with no or very light dc loads, place an RC snubber circuit at the OPAx191 output to reduce any possibility of ringing in lightly-loaded applications. Figure 8-6 illustrates the recommended RC snubber circuit.

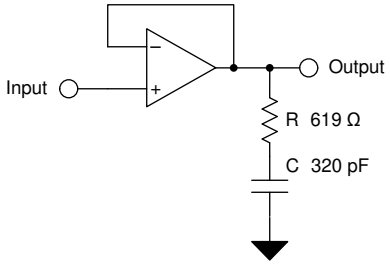


Figure 8-6. RC Snubber Circuit for Lightly-Loaded Applications in Unity Gain

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small, 10-Ω to 20-Ω resistor (R_{ISO}) in series with the output, as shown in Figure 8-7. This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the OPA191 a great choice for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 8-7 uses R_{ISO} to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin. Results using the OPA191 are summarized in Table 8-2. For additional information on techniques to optimize and design using this circuit, TI Precision Design TIPD128, *Capacitive Load Drive Verified Reference Design Using an Isolation Resistor*, details complete design goals, simulation, and test results.

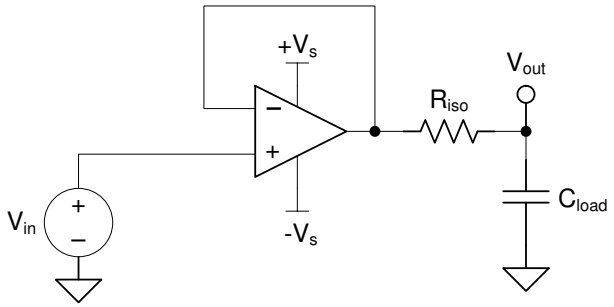


Figure 8-7. Extending Capacitive Load Drive With the OPA191

Table 8-2. OPA191 Capacitive Load Drive Solution Using Isolation Resistor Comparison of Calculated and Measured Results

PARAMETER	VALUE								
Capacitive Load	**100 pF**	**1000 pF**		**0.01 µF**		**0.1 µF**		**1 µF**	
Phase Margin	**45°**	**45°**	**60°**	**45°**	**60°**	**45°**	**60°**	**45°**	**60°**
R_{ISO} (Ω)	280	113	432	68	210	17.8	53.6	3.6	10
Measured Overshoot (%)	23	23	8	23	8	23	8	23	8

8.3.6 Common-Mode Voltage Range

The OPAx191 is a 36-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 8-8. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 3 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.5 V. There is a small transition region, typically (V+) –3 V to (V+) – 1.5 V in which both input pairs are active. This transition region varies modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance are degraded compared to operation outside this region.

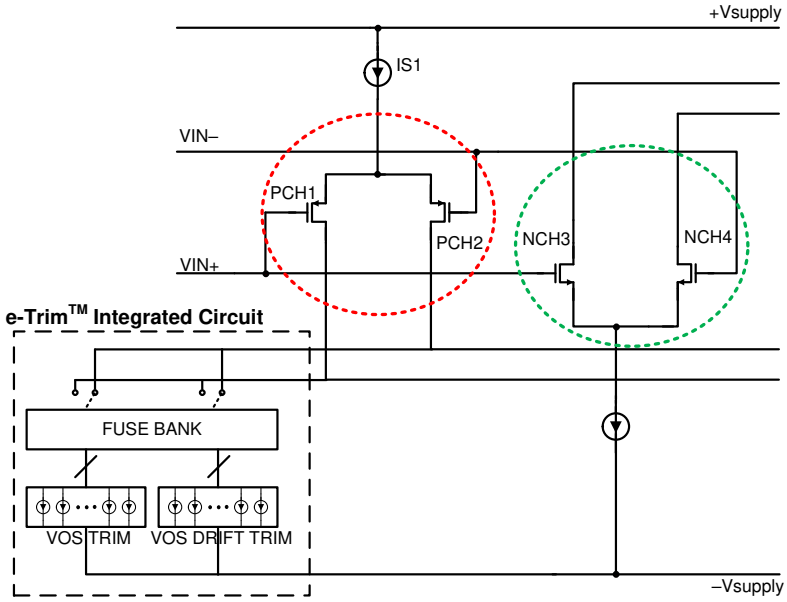


Figure 8-8. Rail-to-Rail Input Stage

To achieve the best performance for two-stage rail-to-rail input amplifiers, avoid the transition region when possible. The OPAx191 uses a precision trim for both the N-channel and P-channel regions. This technique enables significantly lower levels of offset than previous-generation devices, causing variance in the transition region of the input stages to appear exaggerated relative to offset over the full common-mode range, as shown in Figure 8-9.

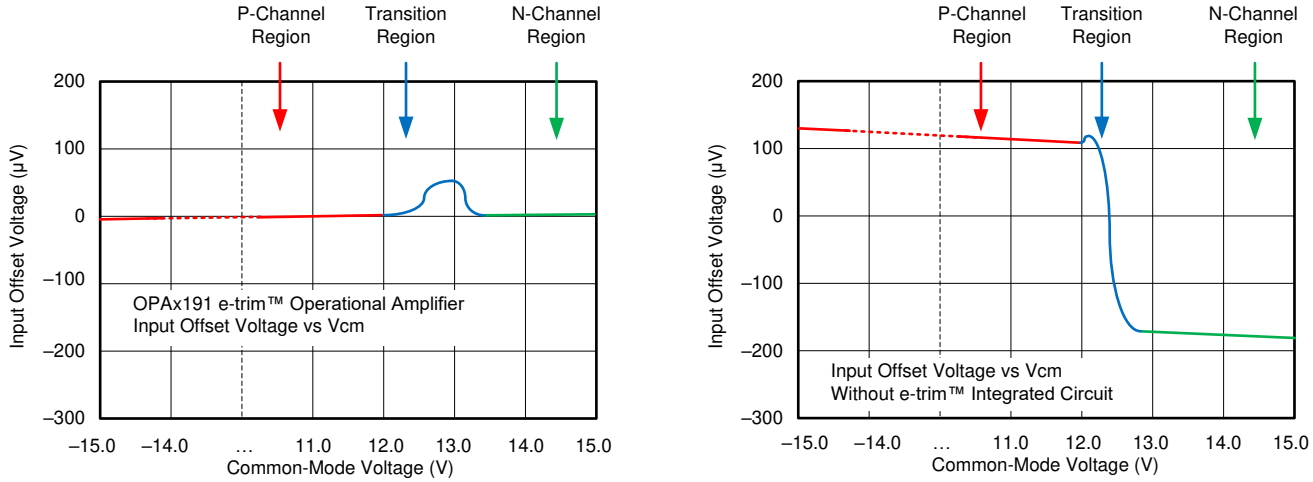


Figure 8-9. Common-Mode Transition vs Standard Rail-to-Rail Amplifiers

8.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See Figure 8-10 for an illustration of the ESD circuits contained in the OPAx191 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

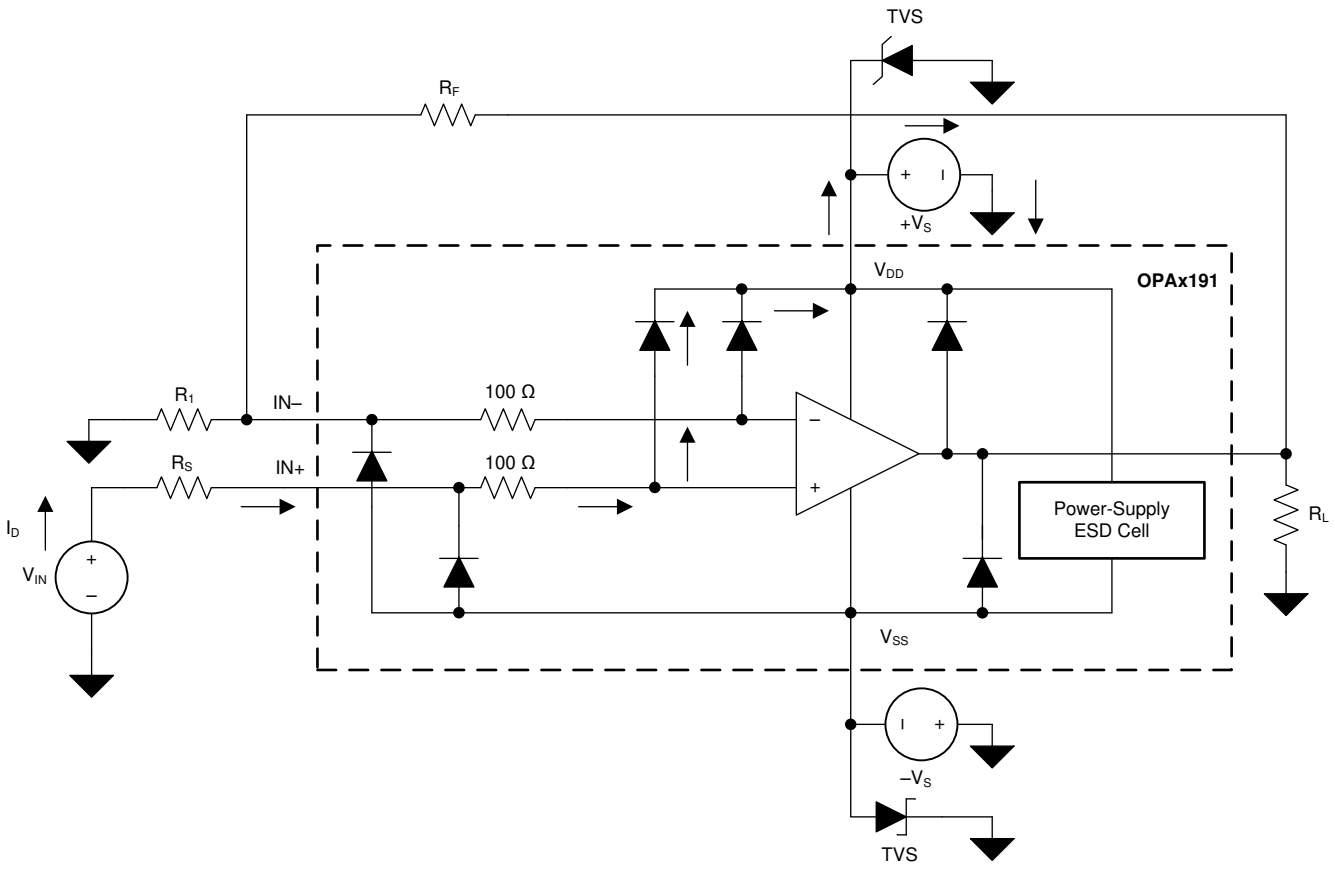


Figure 8-10. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very high voltage for a very short duration (for example, 1 kV for 100 ns); whereas, an EOS event is lower voltage for a longer duration (for example, 50 V for 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit labeled ESD power-supply circuit. The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressor (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

8.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time.

8.4 Device Functional Modes

The OPAx191 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx191 is 36 V (±18 V).

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The OPAx191 family offers outstanding dc precision and ac performance. These devices operate up to 36-V supply rails and offer true rail-to-rail input/output, ultralow offset voltage and offset voltage drift, as well as 2-MHz bandwidth and high capacitive load drive. These features make the OPAx191 a robust, high-performance operational amplifier for high-voltage industrial applications.

9.2 Typical Applications

9.2.1 Low-side Current Measurement

Figure 9-1 shows the OPA191 configured in a low-side current sensing application. For a full analysis of the circuit shown in Figure 9-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0-A to 1-A Single-Supply Low-Side Current-Sensing Solution* .

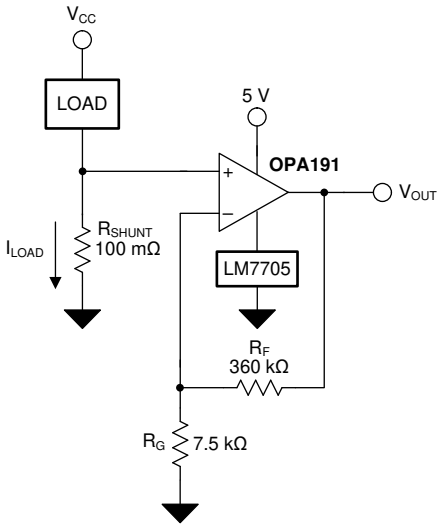


Figure 9-1. OPA191 in a Low-Side, Current-Sensing Application

9.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

9.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 9-1 is given in Equation 2

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{2}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using Equation 3.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \tag{3}$$

Using Equation 3, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPA191 to produce an output voltage of 0 V to 4.9 V. The gain needed by the OPA191 to produce the necessary output voltage is calculated using Equation 4:

$$Gain = \frac{\left(V_{OUT\_MAX} - V_{OUT\_MIN}\right)}{\left(V_{IN\_MAX} - V_{IN\_MIN}\right)} \tag{4}$$

Using Equation 4, the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G. Equation 5 is used to size the resistors, R_F and R_G, to set the gain of the OPA191 to 49 V/V.

$$Gain = 1 + \frac{\left(R_F\right)}{\left(R_G\right)} \tag{5}$$

Choosing R_F as 360 kΩ, R_G is calculated to be 7.5 kΩ. R_F and R_G were chosen as 360 kΩ and 7.5 kΩ because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. Figure 2 shows the measured transfer function of the circuit shown in Figure 9-1.

9.2.1.3 Application Curves

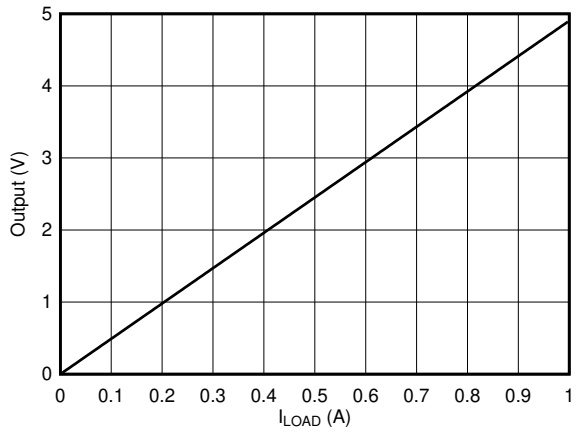


Figure 9-2. Low-Side, Current-Sense, Transfer Function

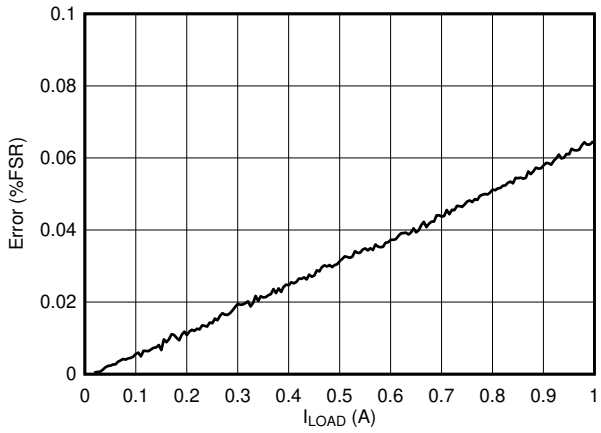


Figure 9-3. Low-Side, Current-Sense, Full-Scale Error

9.2.2 16-Bit Precision Multiplexed Data-Acquisition System

Figure 9-4 shows a 16-bit, differential, 4-channel, multiplexed, data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR), analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front-end, and a 4-channel differential multiplexer (mux). This application example shows the process for optimizing the precision, high-voltage, front-end drive circuit using the OPA191 and OPA140 to achieve excellent dynamic performance and linearity with the ADS8864. The full design can be found in TI Precision Design TIPD151, *16-Bit, 400-kSPS, Four-Channel MUX Data Acquisition System for High-Voltage Inputs*.

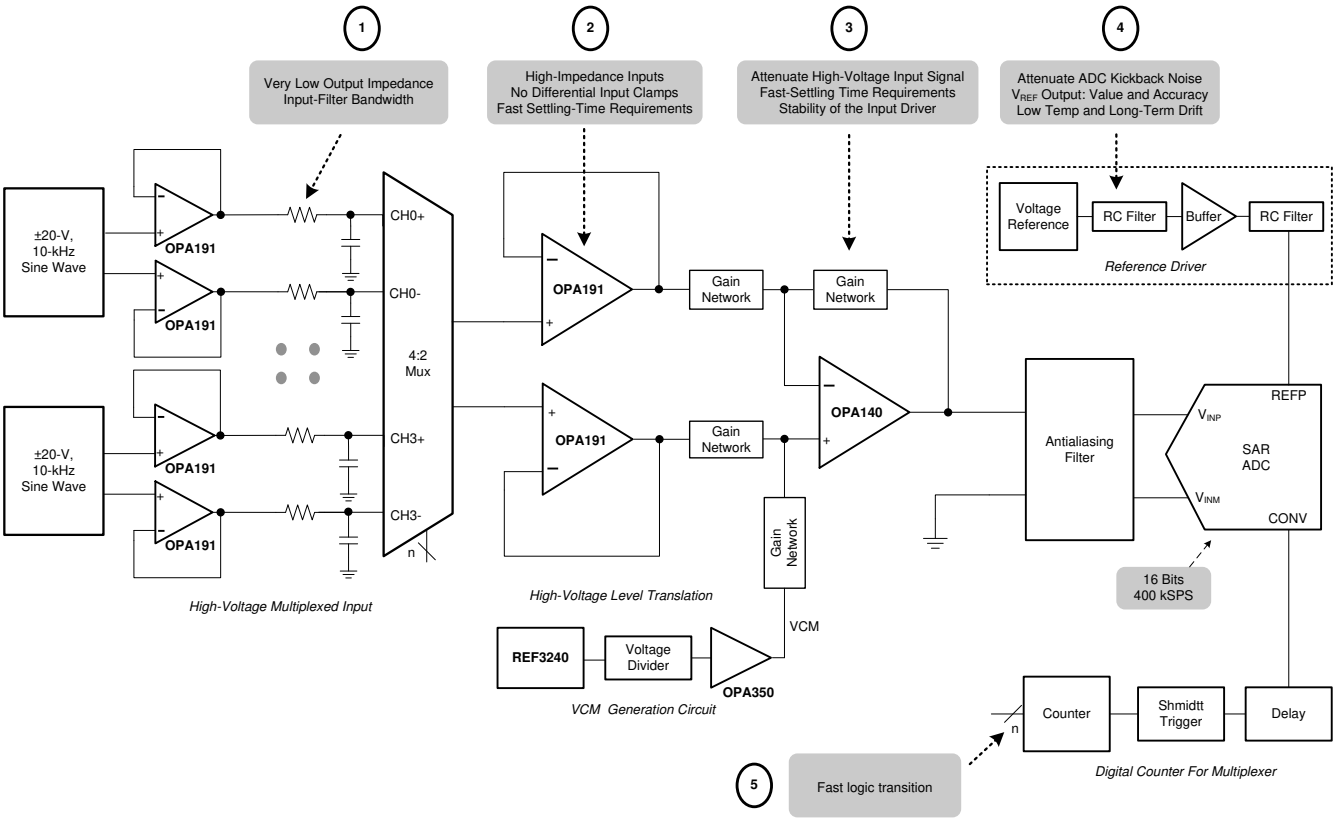


Figure 9-4. OPA191 in 16-Bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High-Voltage Inputs With Lowest Distortion

9.2.2.1 Design Requirements

The primary objective is to design a ±20-V, differential, 4-channel, multiplexed, data acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10-kHz, full-scale, pure sine-wave input. The design requirements for this block design are:

- System supply voltage: ±15 V
- ADC supply voltage: 3.3 V
- ADC sampling rate: 400 kSPS
- ADC reference voltage (REFP): 4.096 V
- System input signal: A high-voltage differential input signal with a peak amplitude of 10 V and frequency (f_{IN}) of 10 kHz are applied to each differential input of the mux.

9.2.2.2 Detailed Design Procedure

The purpose of this application example is to design an optimal, high-voltage, multiplexed, data-acquisition system for highest system linearity and fast settling. The overall system block diagram is shown in Figure 9-4. The circuit is a multichannel, data-acquisition, signal chain consisting of an input low-pass filter, multiplexer (mux), mux output buffer, attenuating SAR ADC driver, digital counter for the mux, and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. The two primary design considerations to maximize the performance of a precision, multiplexed, data-acquisition system are the mux input analog front-end and the high-voltage, level translation, SAR ADC driver design. However, carefully design each analog circuit block based on the ADC performance specifications in order to achieve the fastest settling at 16-bit resolution and lowest distortion system. Figure 9-4 includes the most important specifications for each individual analog block.

This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel. The first step in the design is to understand the requirement for an extremely-low-impedance input-filter design for the mux. This understanding helps in the decision of an appropriate input filter and selection of a mux to meet the system settling requirements. The next important step is the design of the attenuating analog front-end (AFE) used to level translate the high-voltage input signal to a low-voltage ADC input while maintaining the amplifier stability. Then, the next step is to design a digital interface to switch the mux input channels with minimum delay. The final design challenge is to design a high-precision, reference-driver circuit that provides the required REFP reference voltage with low offset, drift, and noise contributions.

9.2.3 Slew Rate Limit for Input Protection

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the OPAx191 make the device an optimal amplifier to achieve slew rate control for both dual-supply and single-supply systems. Figure 9-5 shows the OPA191 in a slew-rate limit design. For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIPD140, *Single Op-Amp Slew Rate Limiter*..

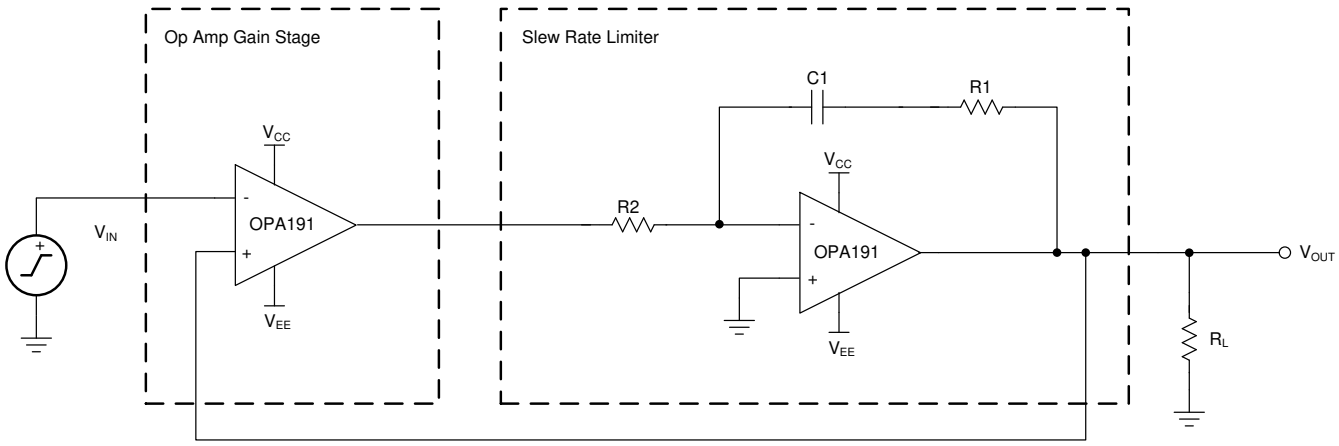


Figure 9-5. Slew Rate Limiter Uses One Op Amp

10 Power Supply Recommendations

The OPAx191 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Section 6.9*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see *Section 6.1*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Section 11*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
  - Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. For more detailed information, refer to *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 11-2, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. After any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

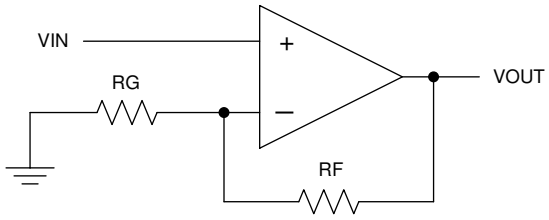


Figure 11-1. Schematic Representation

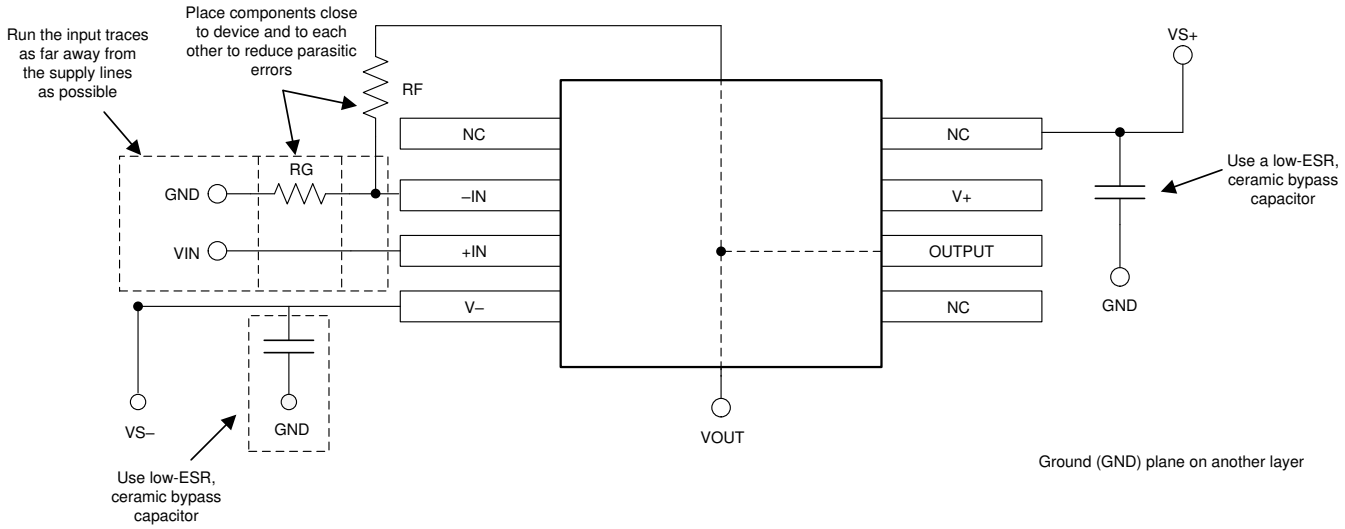


Figure 11-2. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ SImulation Software (Free Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder at http://www.ti.com/tool/tina-ti.

12.1.1.2 TI Precision Designs

TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/, are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

12.2 Documentation Support

12.2.1 Related Documentation

- Texas Instruments, *Circuit Board Layout Techniques*
- Texas Instruments, *Op Amps for Everyone* design reference

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

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Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA191ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA191
OPA191ID.Z	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA191
OPA191IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZAMV
OPA191IDBVR.Z	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZAMV
OPA191IDBVRG4.Z	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZAMV
OPA191IDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZAMV
OPA191IDBVT.Z	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZAMV
OPA191IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZANV
OPA191IDGKR.Z	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZANV
OPA191IDGKRG4.Z	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZANV
OPA191IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZANV
OPA191IDGKT.Z	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZANV
OPA191IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA191
OPA191IDR.Z	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA191
OPA191IDRG4.Z	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA191
OPA2191ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2191
OPA2191ID.Z	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2191
OPA2191IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2191
OPA2191IDGKR.Z	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2191
OPA2191IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2191
OPA2191IDGKT.Z	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2191
OPA2191IDGKTG4.Z	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2191
OPA2191IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2191
OPA2191IDR.Z	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2191
OPA2191IDRG4.Z	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2191
OPA4191ID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4191
OPA4191ID.Z	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4191
OPA4191IDG4.Z	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4191
OPA4191IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4191

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA4191IDR.Z	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4191
OPA4191IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4191
OPA4191IPWR.Z	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4191
OPA4191IPWT	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4191
OPA4191IPWT.Z	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4191
OPA4191IRUMR	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 4191
OPA4191IRUMR.Z	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 4191
OPA4191IRUMRG4.Z	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 4191
OPA4191IRUMT	Active	Production	WQFN (RUM) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 4191
OPA4191IRUMT.Z	Active	Production	WQFN (RUM) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 4191

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

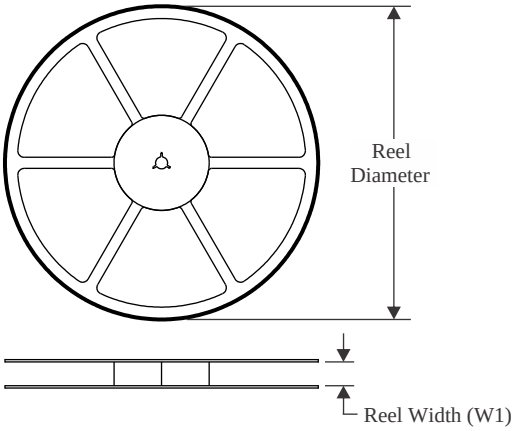
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

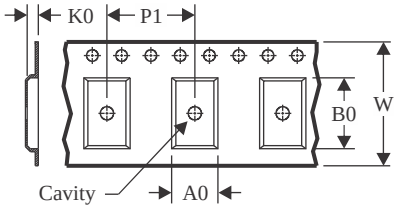
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

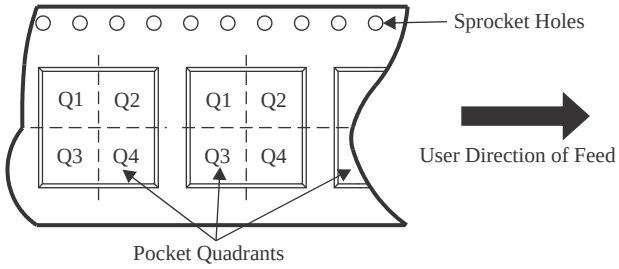


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

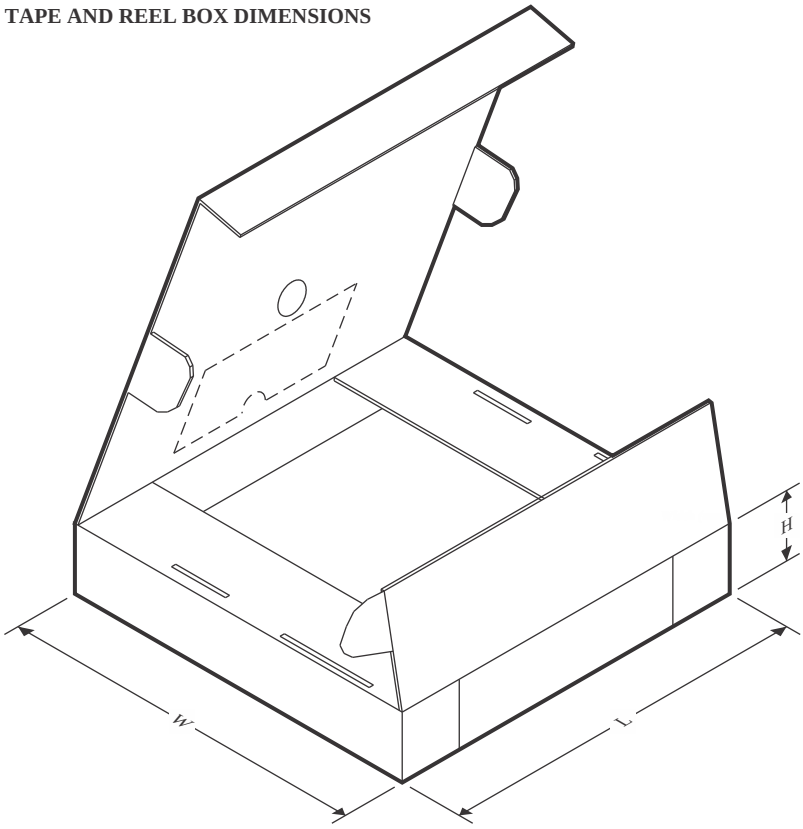
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA191IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA191IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA191IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA191IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA191IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2191IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2191IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2191IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4191IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4191IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4191IPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4191IRUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA4191IRUMT	WQFN	RUM	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

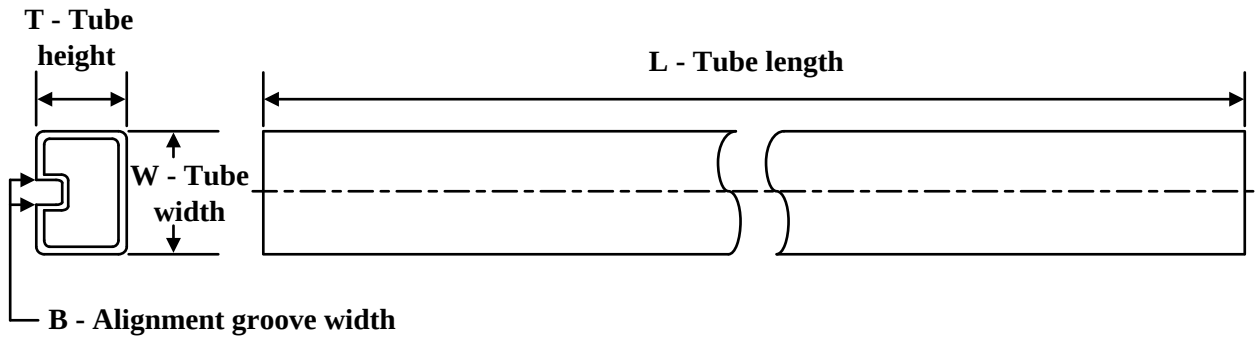
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

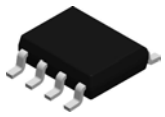
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA191IDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA191IDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA191IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
OPA191IDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA191IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2191IDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2191IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2191IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA4191IDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4191IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
OPA4191IPWT	TSSOP	PW	14	250	210.0	185.0	35.0
OPA4191IRUMR	WQFN	RUM	16	3000	367.0	367.0	35.0
OPA4191IRUMT	WQFN	RUM	16	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA191ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA191ID.Z	D	SOIC	8	75	506.6	8	3940	4.32
OPA2191ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2191ID.Z	D	SOIC	8	75	506.6	8	3940	4.32
OPA4191ID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4191ID.Z	D	SOIC	14	50	506.6	8	3940	4.32
OPA4191IDG4.Z	D	SOIC	14	50	506.6	8	3940	4.32

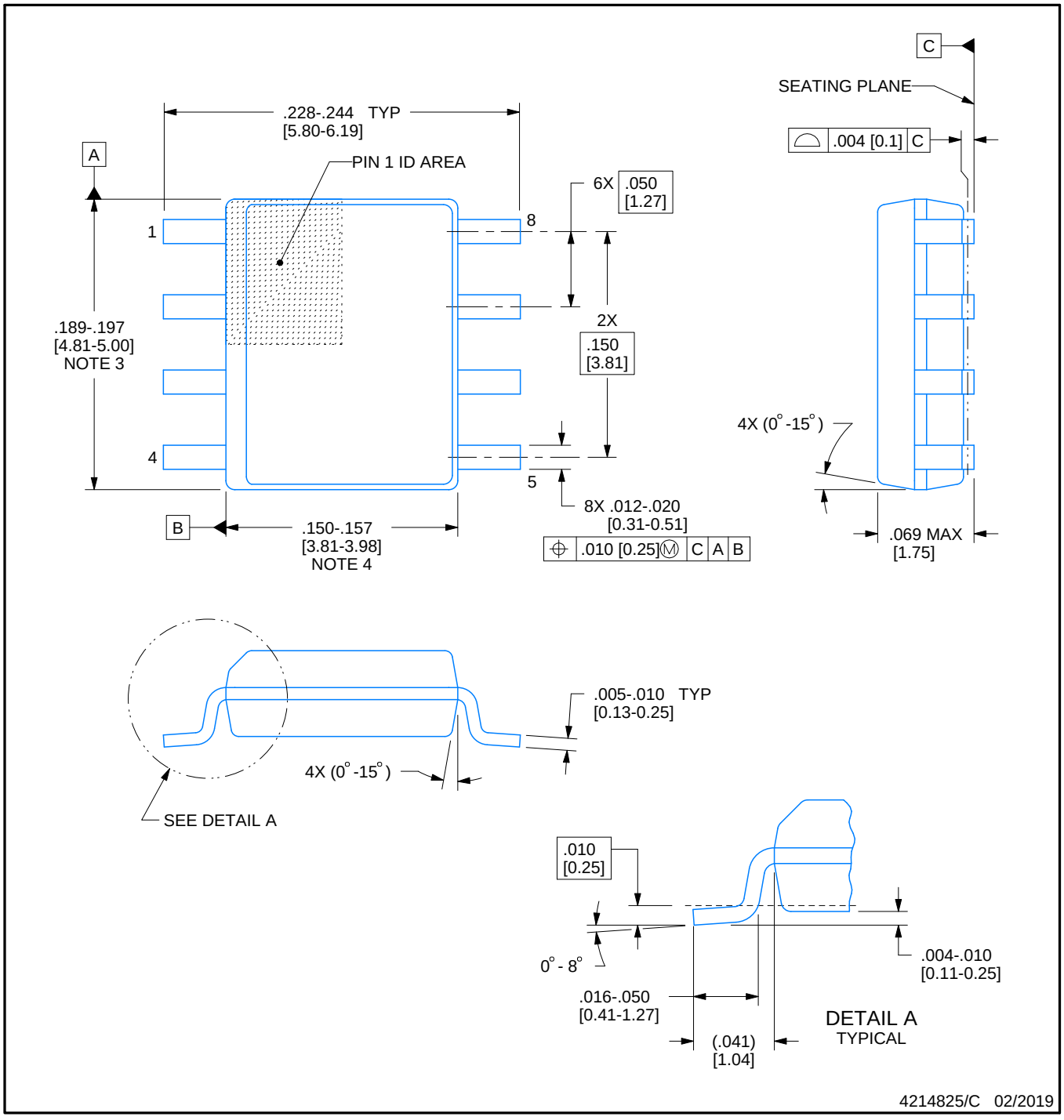


PACKAGE OUTLINE

D0008A

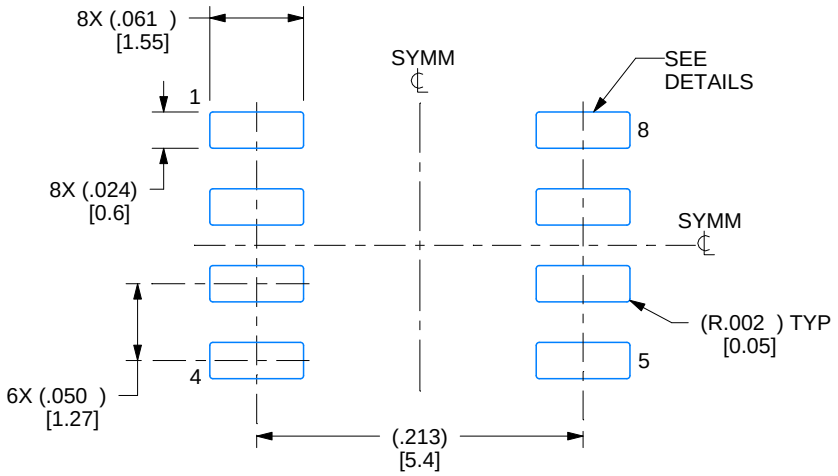
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

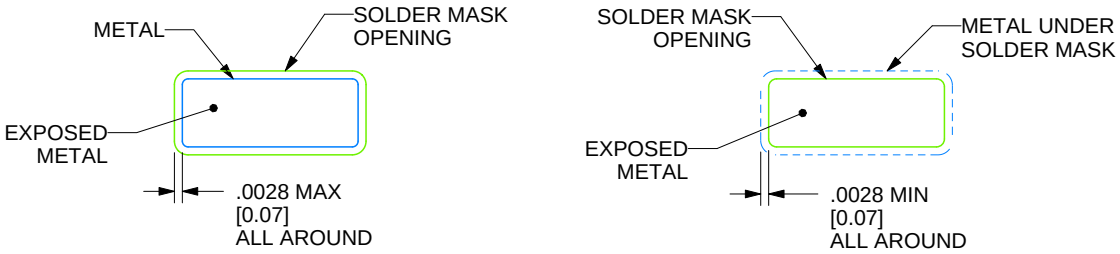


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

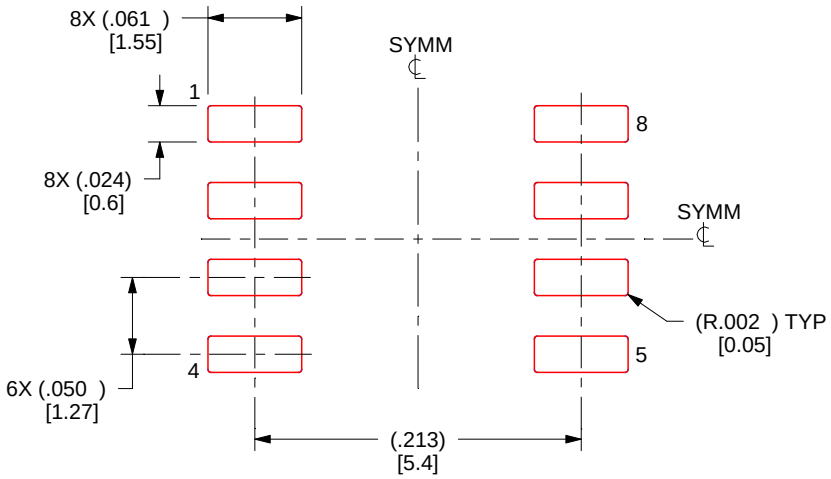
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

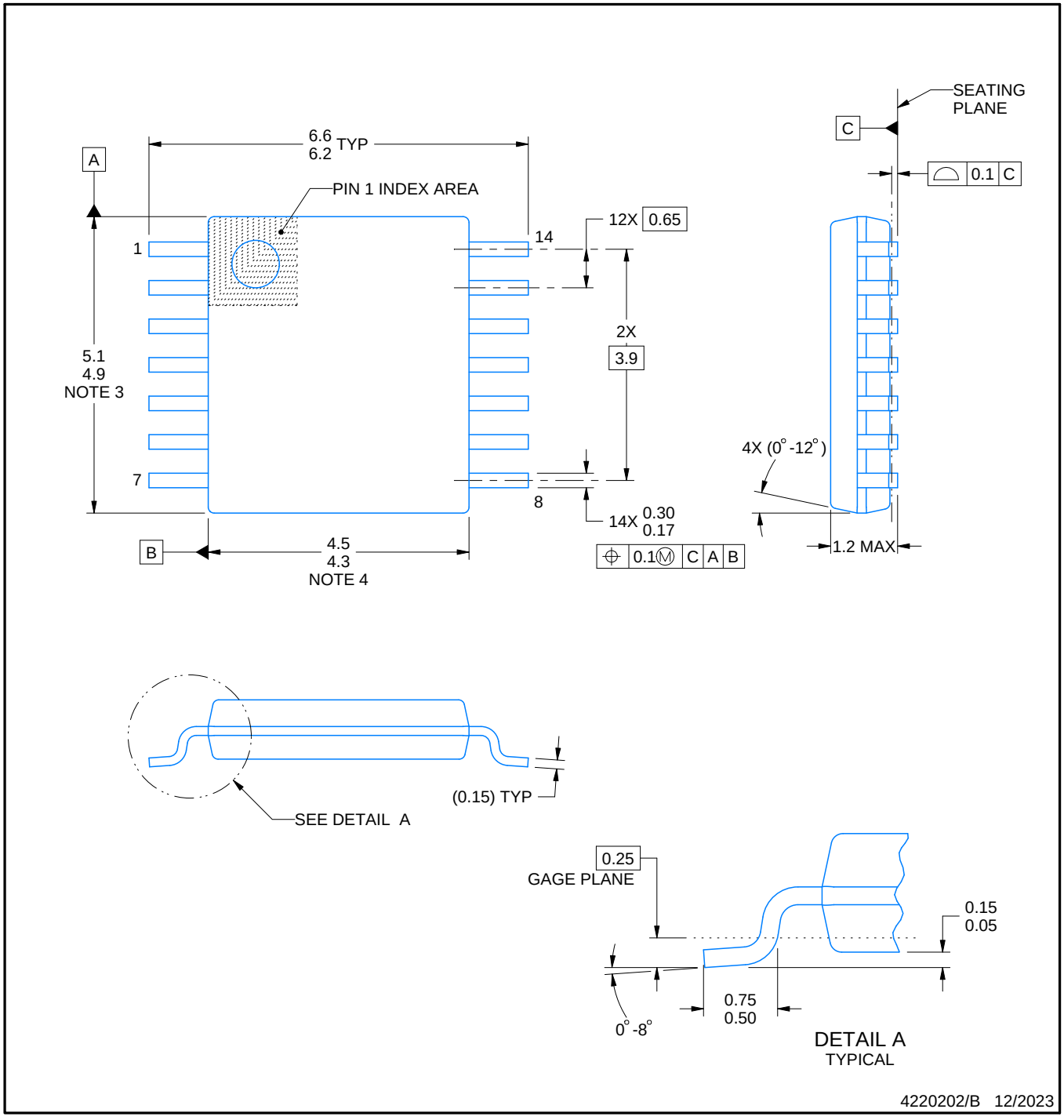
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

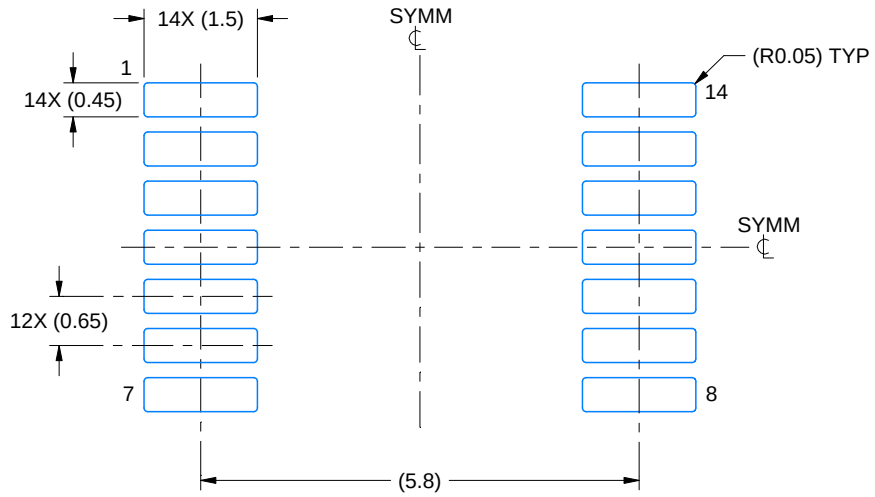
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

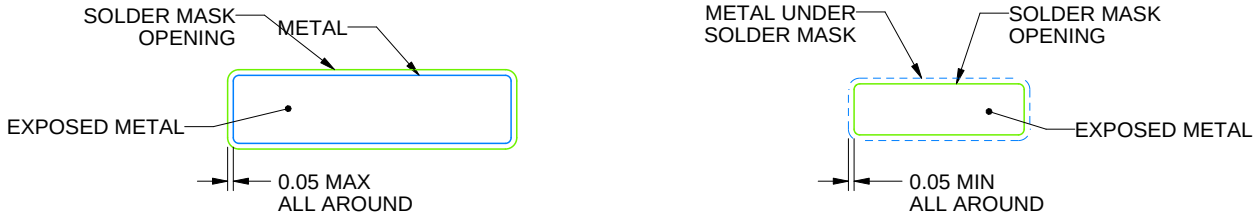


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

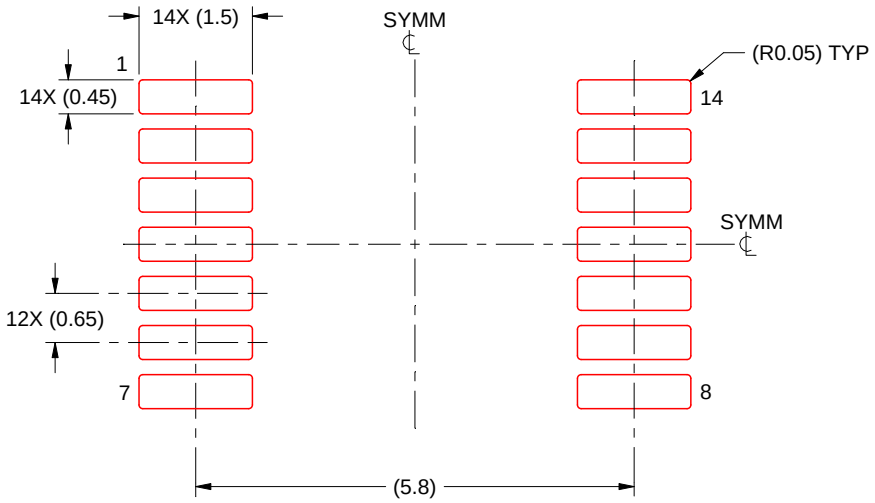


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

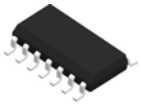


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

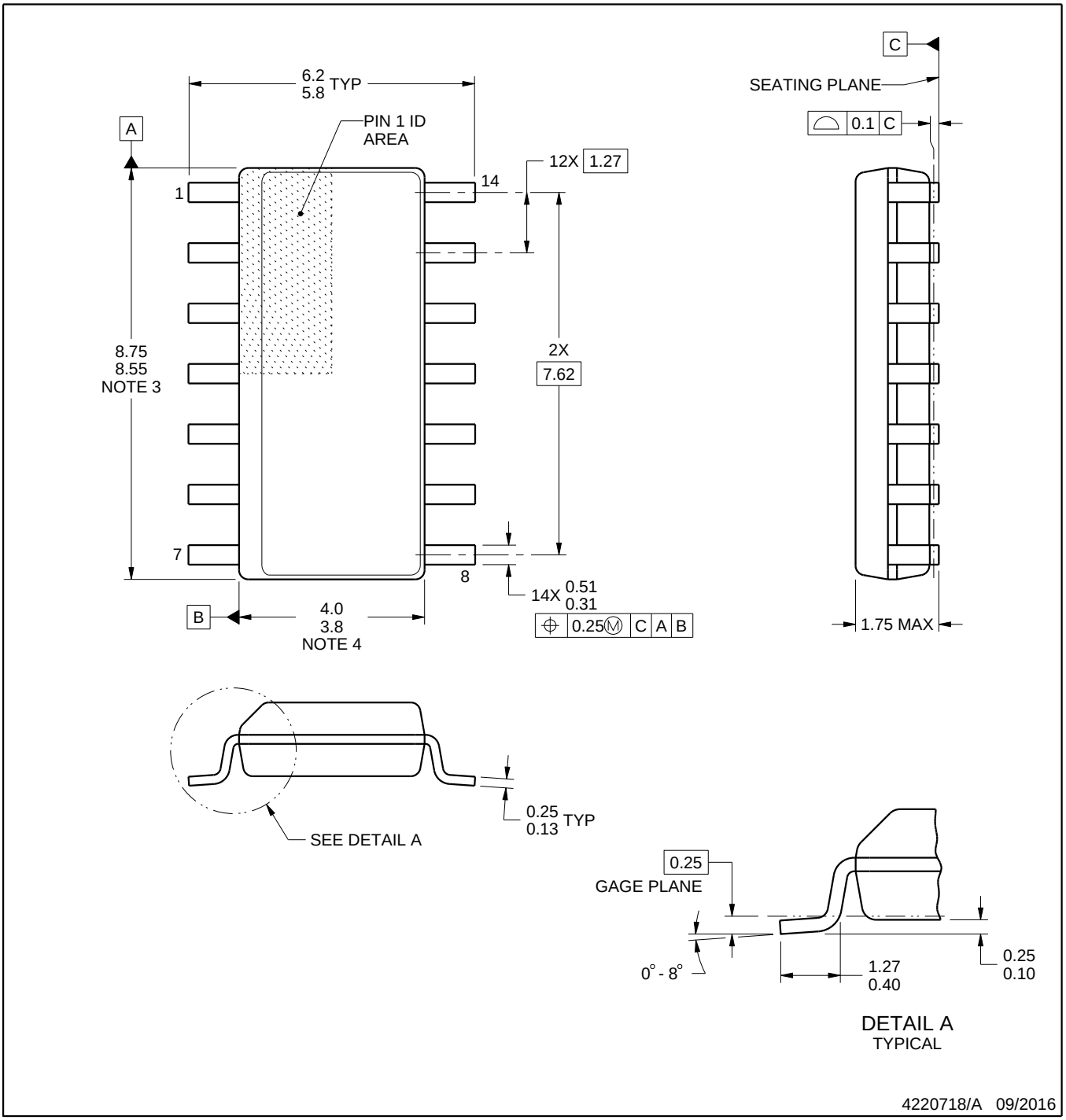


PACKAGE OUTLINE

D0014A

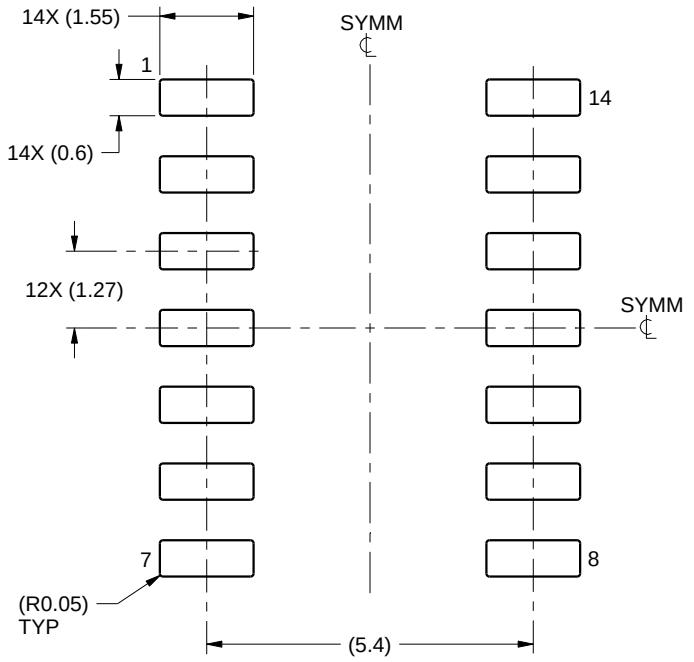
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

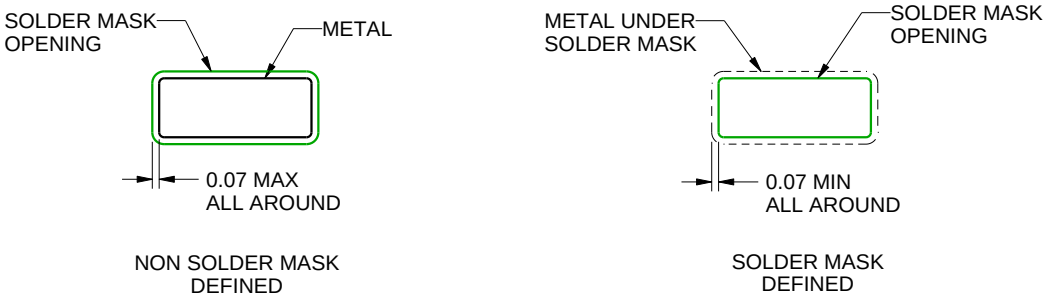


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

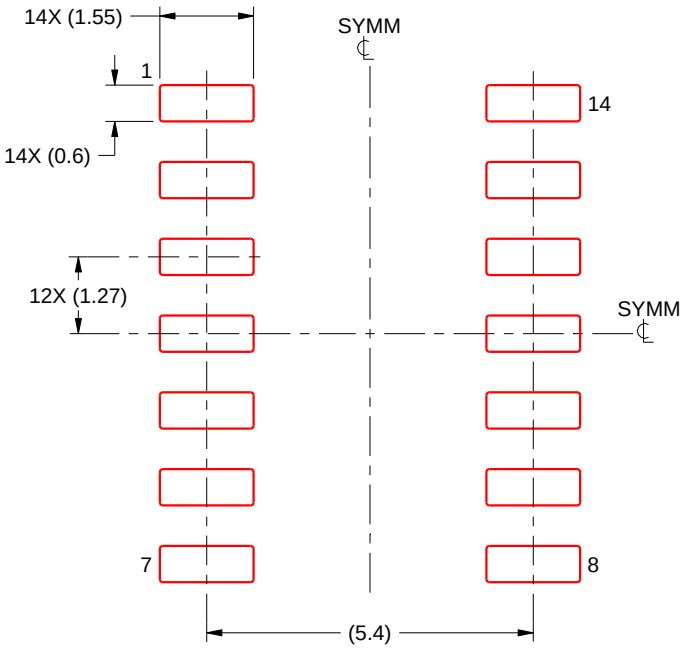
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

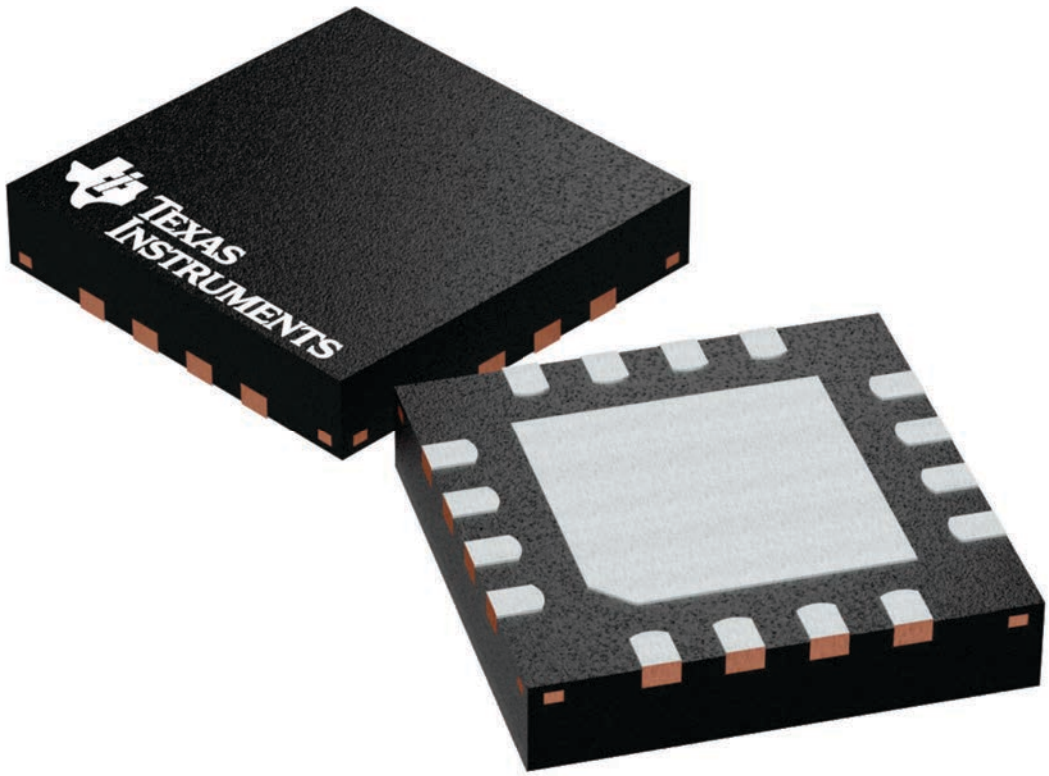
RUM 16

WQFN - 0.8 mm max height

4 x 4, 0.65 mm pitch

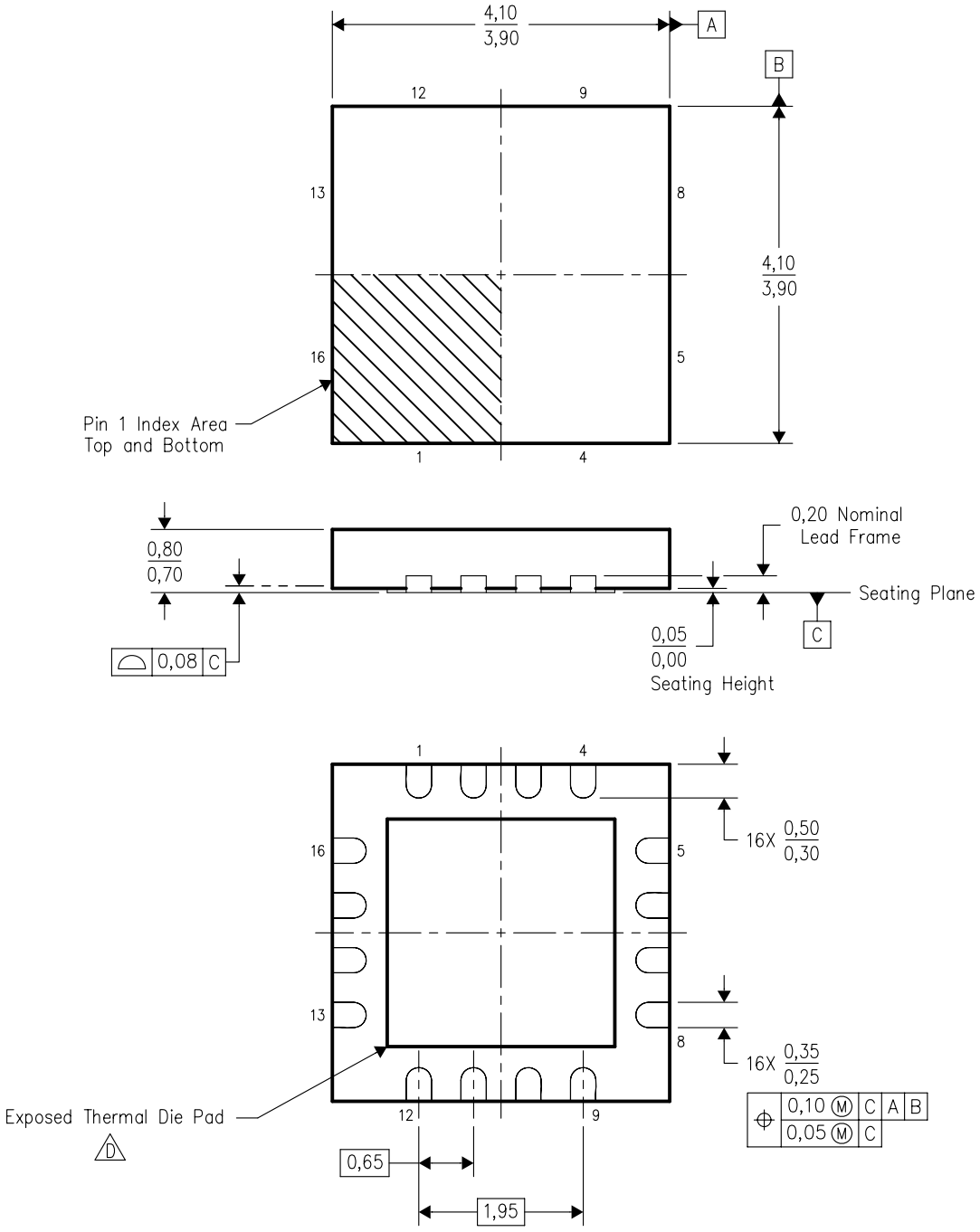
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224843/A

RUM (S–PQFP–N16) PLASTIC QUAD FLATPACK



4209092/A 10/2007

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220 variation WGGC–3.

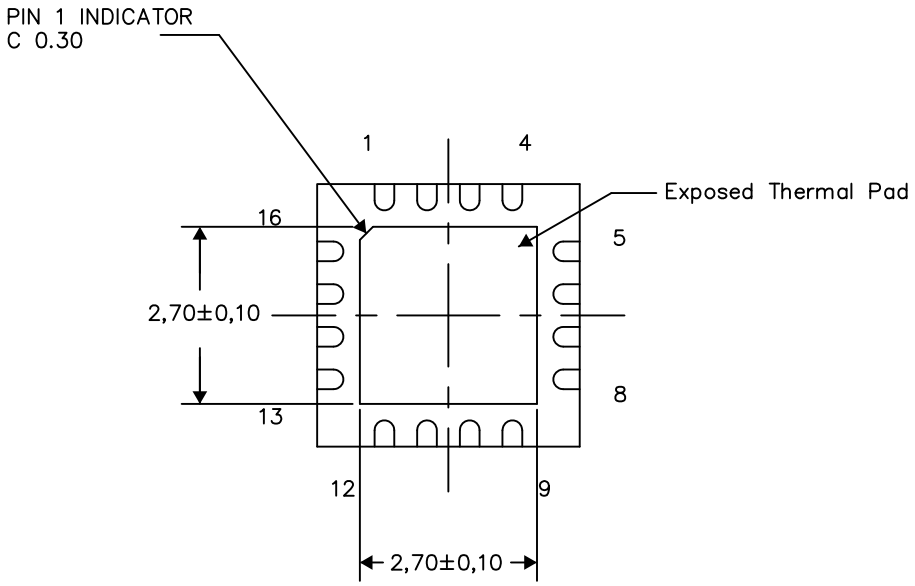
RUM (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4209093–2/F 09/15

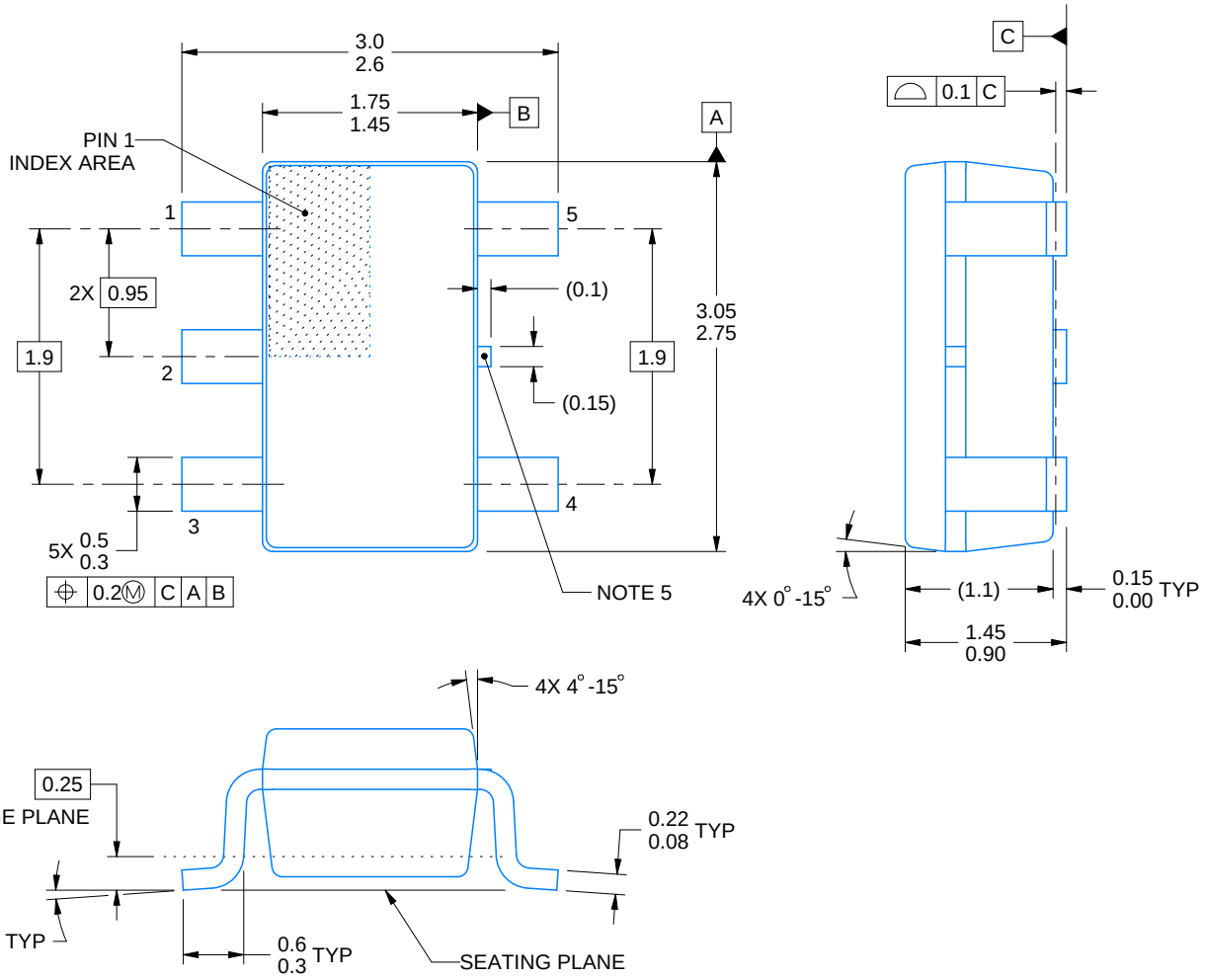
NOTES: All linear dimensions are in millimeters

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

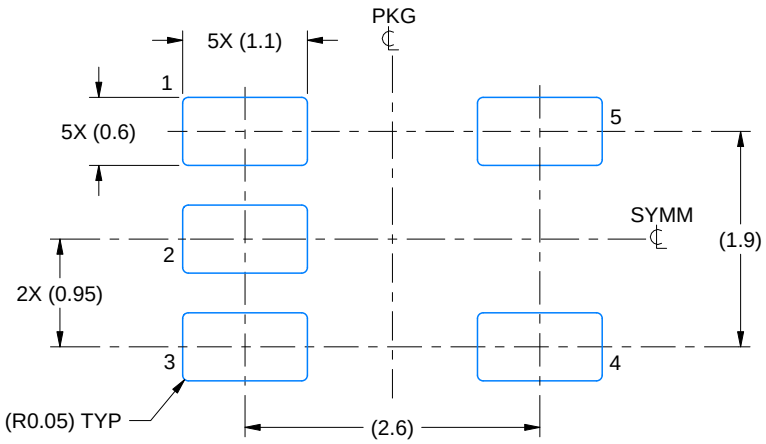
SMALL OUTLINE TRANSISTOR



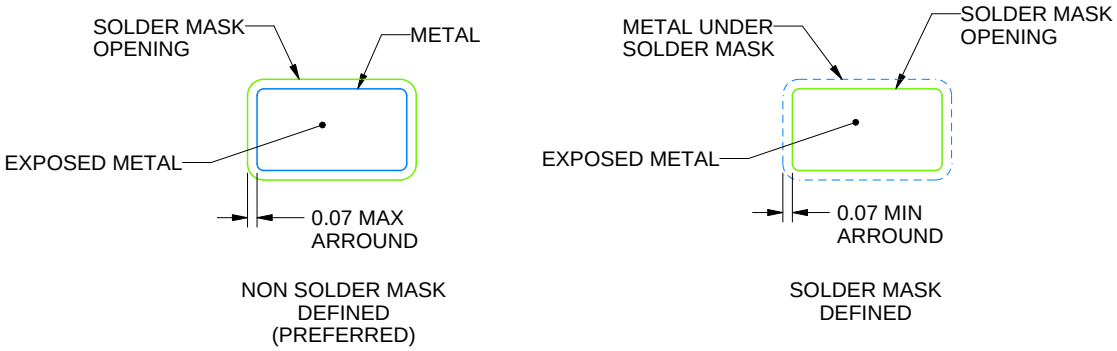
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

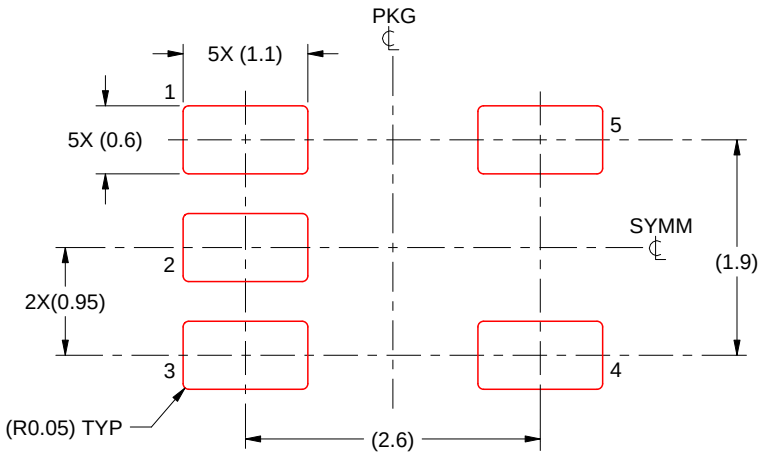


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

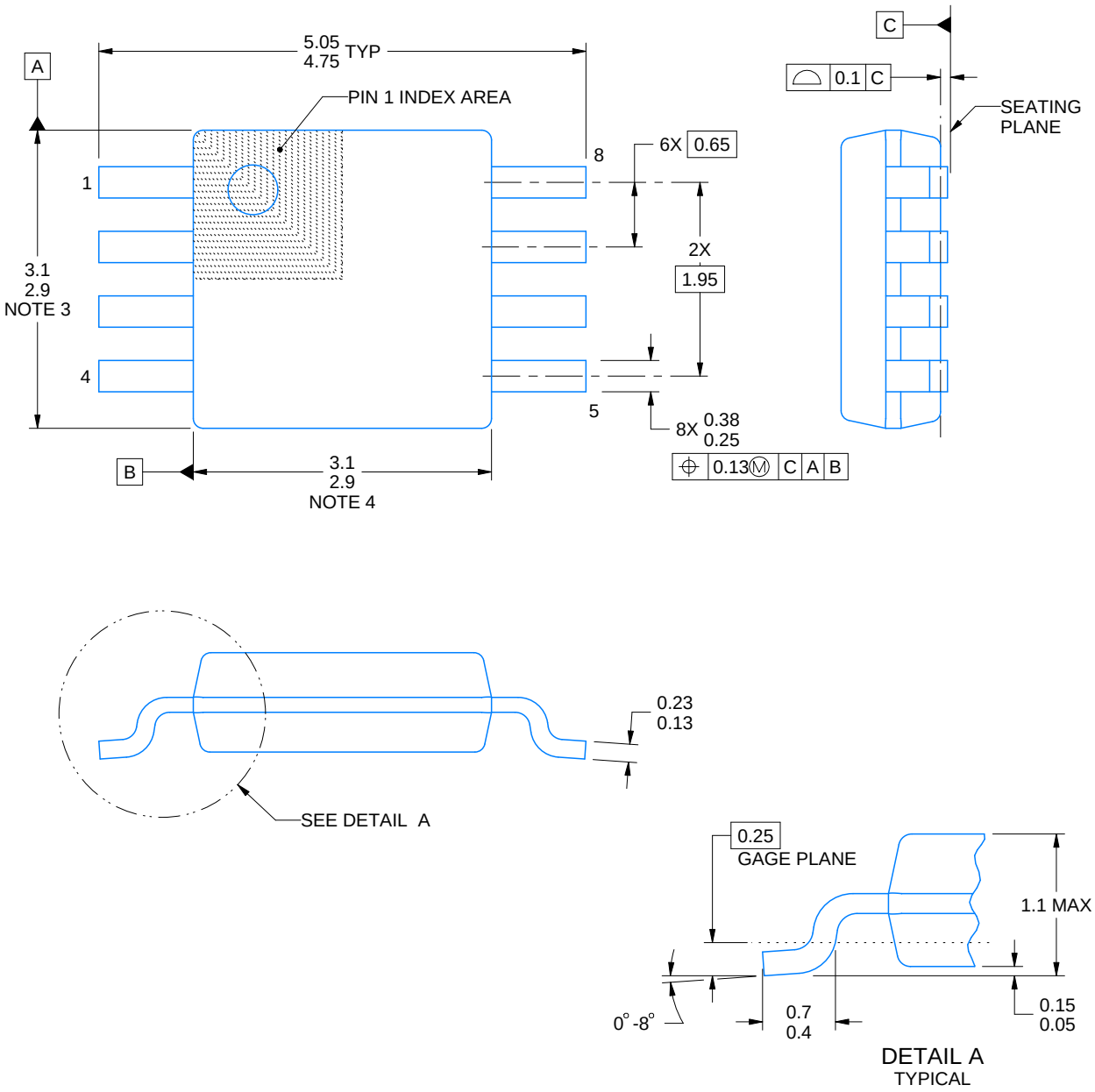
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

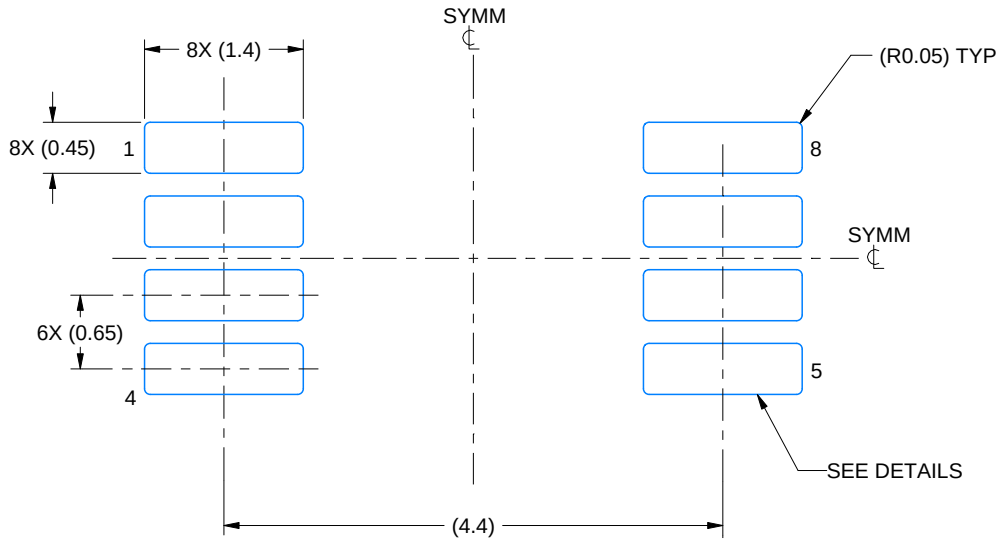
SMALL OUTLINE PACKAGE



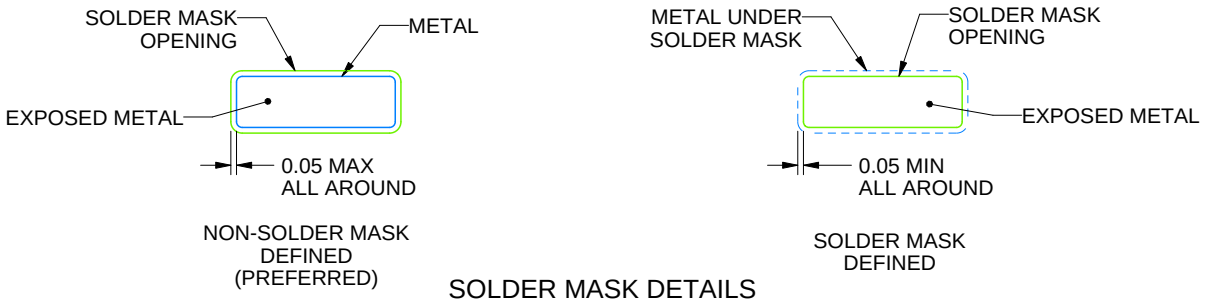
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

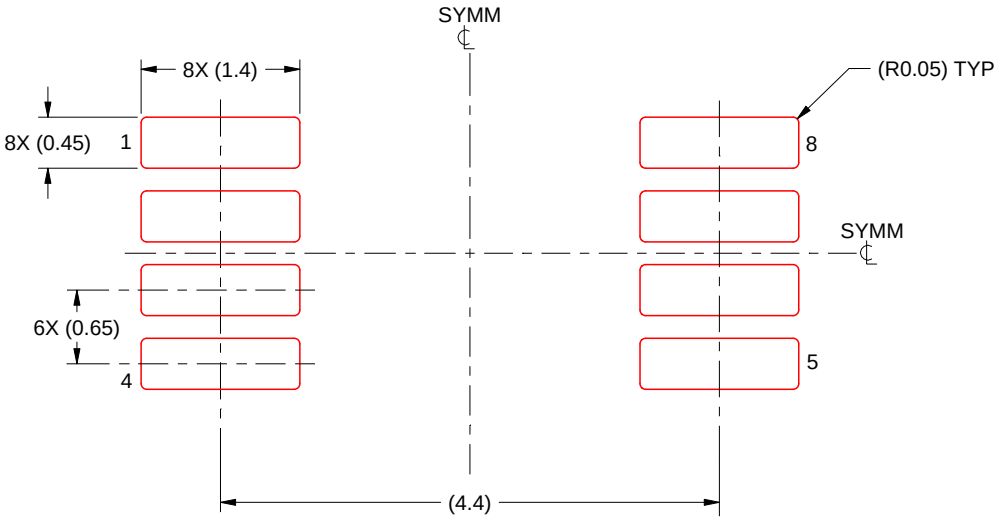


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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